UNIVERSITY OF CALIFORNIA
RIVERSIDE

Two-Dimensional Materials Preparation, Characterization and Device Integration for Novel Applications

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Materials Science and Engineering

by

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March 2020

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Acknowledgements

I would like to thank everyone who played a role in my academic accomplishments. All lab members of the Bartels' Lab, old and new, for teaching me the skills I truly need to work as a leader. My behind-the-scenes support, my parents, who were crucial to every aspect of my successes. My committee members for your guidance and unwavering support. The CCDC Army Research Laboratory Adelphi, MD for your financial and academic support to complete my Ph.D.

Lastly, to my oldest friends and new ones I have made along the way, without whom, I would have lost myself long ago. All your genuine love, enthusiasm, and support throughout my degree astounds me and will forever.

ABSTRACT OF THE DISSERTATION

Two-Dimensional Materials Preparation, Characterization
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by

Michael Daniel Valentin

Doctor of Philosophy, Graduate Program in Materials Science and Engineering
University of California, Riverside, March 2020
Dr. Ludwig Bartels, Chairperson

Two-dimensional materials, especially transaction metal dichalcogenides, have shown a wide variety of applications and variability of desirable electronic characteristics. Various methods have been demonstrated to deposit pristine monolayer flakes. Traditional chemical vapor deposition at atmospheric and high-vacuum pressure growth of TMDs had been demonstrated. Rhenium disulfide (ReS_2), a novel TMD, is grown via chemical vapor deposition and tested a variety of methods concluding with results and challenges to come.

In this work, TMD thin films have proven to play a key role in advancing performance and high-power devices. Vertical devices based on 2D semiconductor heterostructures demonstrate the potential for high speed and large power performance.

Taking advantage of mainstream 3D materials such as GaN and novel 2D materials such as transition metal dichalcogenides to fabricate this structure. The path to a functionable 3-terminal heterojunction bipolar transistor (HBT) has been revealed showing that clean, sharp interfaces play a major role in the electrical performance of proposed devices.

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Introduction

Motivation

Recent discoveries have brought a lot of attention to two-dimensional materials. Graphene[1, 2], a single sheet of carbon atoms, offers high mobility[3] and rich physics.[4]

Graphene has outstanding conductivity, which promised a revolution to the semiconductor industry.[1] Unfortunately, graphene has no native band gap rendering it unsuitable for the fabrication of transistors. There are various tricks to turn graphene into a semiconductor, though they have detrimental effects.[5]

Transition metal dichalcogenides (TMDs) are another class of materials that can be thinned to a single layer. A single layer of molybdenum disulfide (MoS_2, a typical TMD) consists of a hexagonal flat array of molybdenum atoms that are covered above and below by hexagonal flat arrays of sulfur atoms. Bulk MoS_2 interacts between the sulfur-sulfur planes of each layer via van der Waals interactions. TMDs are natively indirect band gap semiconductors, but at the single layer, their band gap widens and becomes direct, i.e. suitable for optoelectronic applications.[6] A defining property of TMDs is the wide range of optical band gaps available from 1.1eV to 1.9eV ($MoTe_2$ to WS_2). TMDs can complement the properties of graphene through their emergence of strong photoluminescence (PL) in the monolayer, high mobility and carrier concentrations[7], and in some cases, spin-orbit coupling.[8] TMDs exhibit superior mechanical flexibility due to their thin structure compared to silicon.[9] These properties give TMDs great potential for

next generation electronics that have excellent durability due to their thinness and the ability to endure high mechanical strain that is reversible[10, 11], similar to a sheet of paper compared to a plywood board.

Although monolayer TMD material is optimal for the maximum thinning of future electronics, synthesis of purely homogenous films is challenging. Rhenium disulfide (ReS_2) is a novel TMD that maintains a direct band gap in multiple layers due to the electronic decoupling between layers.[12] This provides great promise for facile synthesis of TMDs in industry while maintaining the low temperature aspect coveted by other monolayer TMDs. In this work, synthesis and electrical characterization of rhenium disulfide (ReS_2) are investigated.

Thin film TMD semiconductors have many distinctive properties that make them attractive for various device concepts. Although a large part of the electron device community is attracted to TMDs for their direct band gap, low power, and high on/off ratios, recently TMDs have proven to play a key role in advanced performance, high power devices.[13, 14] Vertical devices based on 2D semiconductor heterostructures have the potential for high speed and large power performance due to large current cross-sections from short current paths. One could take advantage of mainstream 3D materials to create 2D/3D heterostructures using both unique 2D atomically sharp crystals and 3D semiconductors as well.[15]

Chapter 1: Synthesis/Preparation, Device Fabrication, and Characterization

Synthesis and Preparation

Exfoliation

Thin film TMD research for semiconductor application started soon after the isolation of graphene in 2004.[16] TMD layers can be isolated with a myriad of techniques. The first, most common way is the top-down technique: exfoliation. Top-down methods like exfoliation are great research tools but not feasible in industry. Mechanical exfoliation has been the primary method of isolating single-layer 2D materials. This method uses a simple piece of scotch tape to isolate monolayer material from a bulk, highly crystalline sample. This method is not reliable for isolating monolayer TMDs and is irreproducible, taking many samples and time to find pristine monolayer material. When a monolayer island is found, it is usually of the best quality with sharp Raman spectra and bright photoluminescence indicating the closest one can get to an ideal sample. Despite its shortcomings, mechanical exfoliation has proven to be a great research tool to isolate high quality materials synthesized by techniques such as chemical vapor transport (CVT). CVT is a slow yet powerful method to create high quality crystals of materials. A CVT growth of a few grams of high quality 2D materials takes weeks to months requiring consistently high temperatures of 1000-1200˚C.[17]

In efforts to obtain larger amounts of monolayer material, a liquid exfoliation method was developed. In the case of MoS_2, a common process is to take CVT material and dissolve it in a powerful solvent, such as N-meythyl-2-pyrrolidone (NMP).[18] With sonication, sheets of MoS_2 will break off their van der Waals (vdW) forces to the main crystal, suspending them in solution. This liquid exfoliation technique can also play a large part of using 2D materials in applications such as inkjet printing. Printing unique functioning circuits with relative ease and speed. The biggest challenge in this field is 2D sheets of TMD material were found to roll up into 1D nano-rods.[19]

Chemical Vapor Deposition (CVD)

Chemical Vapor Deposition (CVD) is a method commonly used in the semiconductor industry. In the process of CVD, a thin film is formed by either decomposition of a reagent or a reaction of multiple gaseous components. In either case, thin film reactions are typically deposited directly on the surface of a wafer where the reaction is catalyzed. There are multiple types of CVD used in industry such as atmospheric pressure (CVD or APCVD), plasma-enhanced (PECVD), low pressure (LPCVD)[20], and more recently liquid metal organic precursor (MOCVD). In our methods to create TMD material, we use atmospheric pressure CVD for the simplicity of the system and high reproducibility of islands and high-vacuum CVD for homogeneous substrate-scale films, which is a novel growth mechanism developed in the Bartels' lab.[21-26]

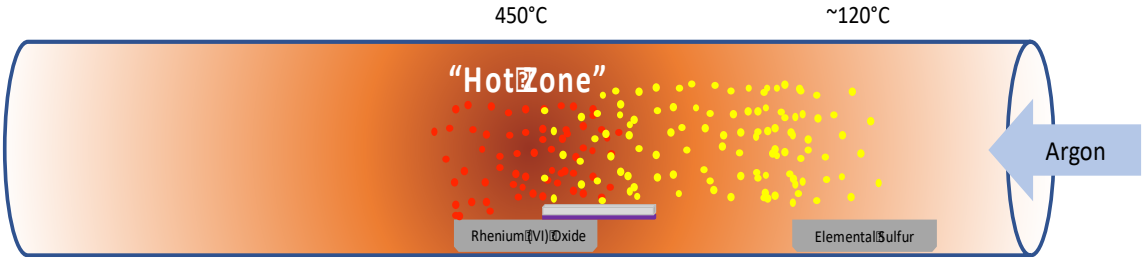

Figure 1.1: Typical TMD chemical vapor deposition (CVD) tube furnace setup. Metal oxide powder is placed in an alumina crucible at the center of the single zone tube furnace where maximum temperature will be reached. A growth substrate is then placed on or near the metal oxide powder boat. Chalcogen powder is placed further upstream due to the lower melting point of the average chalcogen so the radiant heating from the single zone tube furnace melts the chalcogen during growth times. An inert carrier gas facilitates the reaction.

Thin TMD films are favorable material candidates for continuing to scale down semiconductor devices, especially MoS_2 and WSe_2, which are natively *n*- and *p*- doped respectively.

High Vacuum CVD (filament growth)

The International Technology Roadmap for Semiconductors[27] requires the ability to deposit high-quality channel material after initial patterning of the silicon-based substrate. 2D TMDs, such as MoS_2 and WSe_2, offer thin channels with reduced surface scattering making them appealing. Growth of high-quality films have been demonstrated in tube furnace chemical vapor deposition (CVD), metal-organic CVD, liquid exfoliation, and atomic layer deposition (ALD). However, these techniques typically include undesirable reactants that industrial semiconductor companies refrain from using, such as chlorides, oxide-based transmission metal powders, sulfides, and high vapor pressure carbonyls. Ideally, deposition methods produce high-quality homogeneous films at any thickness and full wafer coverage while avoiding particulate contamination or process hazards. Requirements such as these led to the construction of a high-

vacuum MoS_2 chamber that would use pure metal and a volatile liquid-phase precursor. In Table 1.1 we outline the benefits of high vacuum growth process over a tube furnace.

Tube Furnace	High Vacuum
Micron-scale Islands/ defined orientations	Continuous Film
Film in 100μm range	Substrate size film
650ºC – 850ºC	620ºC
Central oxide region	Particulate free
3-4 hours	20 minutes

Table 1.1: Pros/Cons list of CVD via tube furnace vs. High-Vacuum. In a tube furnace synthesis, triangular islands of single crystal, several microns wide MoS_2 is formed. Single crystal films are advantageous for research purposes. In some cases, these triangles coalesce into a film that can span hundreds of microns at most. Both methods of growing are fairly high temperature processes requiring greater than 600°C. High vacuum has the advantage of being homogenous, particulate free, and quicker growth.

In this vacuum chamber we use a set of metallic molybdenum wires at a thickness of 1 mm as the molybdenum source. These are obtained commercially from Alfa Aesar. They are sandwiched between two machined molybdenum plates that are connected to copper rods which lead to an external power supply. Heating of the filaments occurs by passing a high current through them: slowing raising the power supply to ~80A and ~4V, the molybdenum wires become white hot with an estimated temperature of 1800°C. Since the melting point of molybdenum is ~2600°C, evaporation of the molybdenum wires would not occur. For the time being, we use CS_2 (Sigma Aldrich) as our volatile liquid-phase

precursor that we will introduce via a leak valve on our vacuum chamber. Experiments by a previous lab researcher had shown benzenethiol (C_6H_5-SH) to be an ineffective sulfur source for our desired growth process. Although sulfur is double bonded to the carbon in carbon disulfide, process temperatures where we expect the reaction to take place will be well over activation energies for dissociation.

Once a base pressure of high-vacuum ($5x10^{-7}$ torr) is achieved, we first increase our substrate heater to the desired growth temperature of ~650°C depending on the substrate used. Next, a background pressure of CS_2 of ~$5x10^{-4}$ torr is set by a leak valve balance the desired stoichiometry of Mo:S. As described above, the molybdenum wires are resistively heated to process temperatures where we take advantage of the differences in volatility between the molybdenum's melting temperature of 2600°C and MoS_2 that has a much lower melting point of 1180°C. Figure 1.2 shows a diagram of the chamber growth, Figure 1.3 shows the sample holder, while Figure 1.4 shows a grown sample.

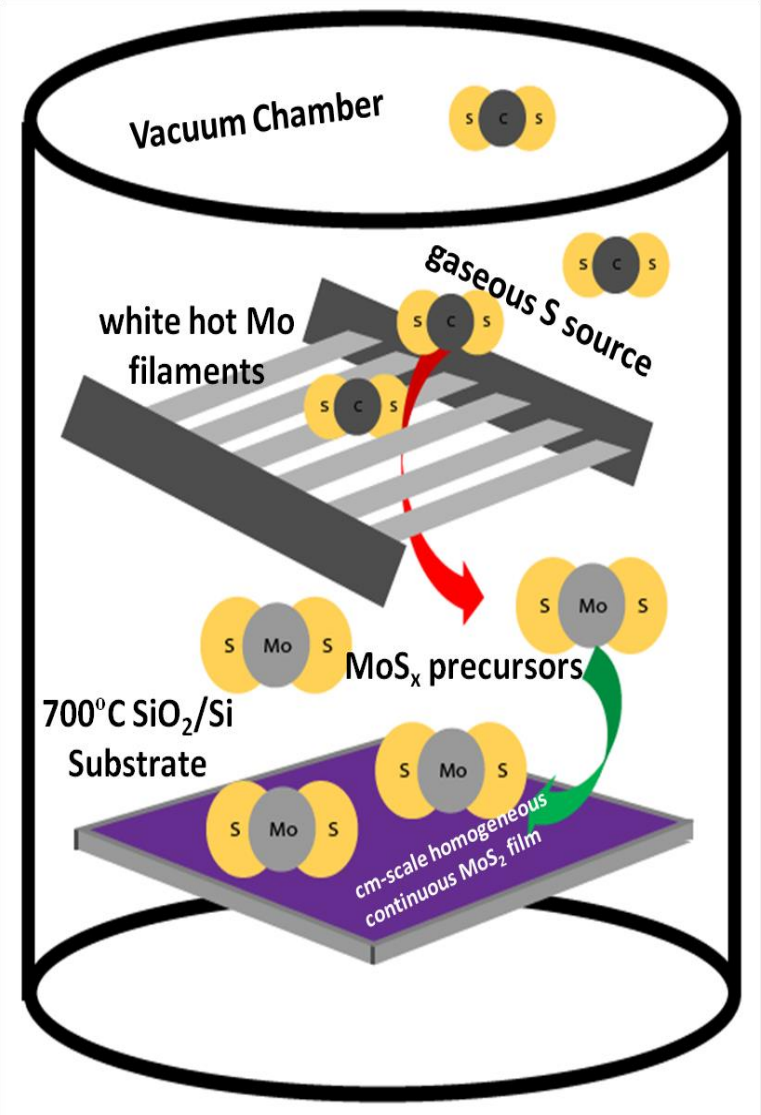

Figure 1.2: Schematic of the MoS_2 High Vacuum Growth Chamber. Vaporized carbon disulfide reacts with the resistively heated molybdenum filaments to synthesize MoS_2 which deposited everywhere around the chamber. The heated sample holder helps to form crystalline, homogenous MoS_2 films on the substrate.

Figure 1.3: The heated sample holder is also made of molybdenum wire. Desired temperatures for SiO_2/Si is 650°C.

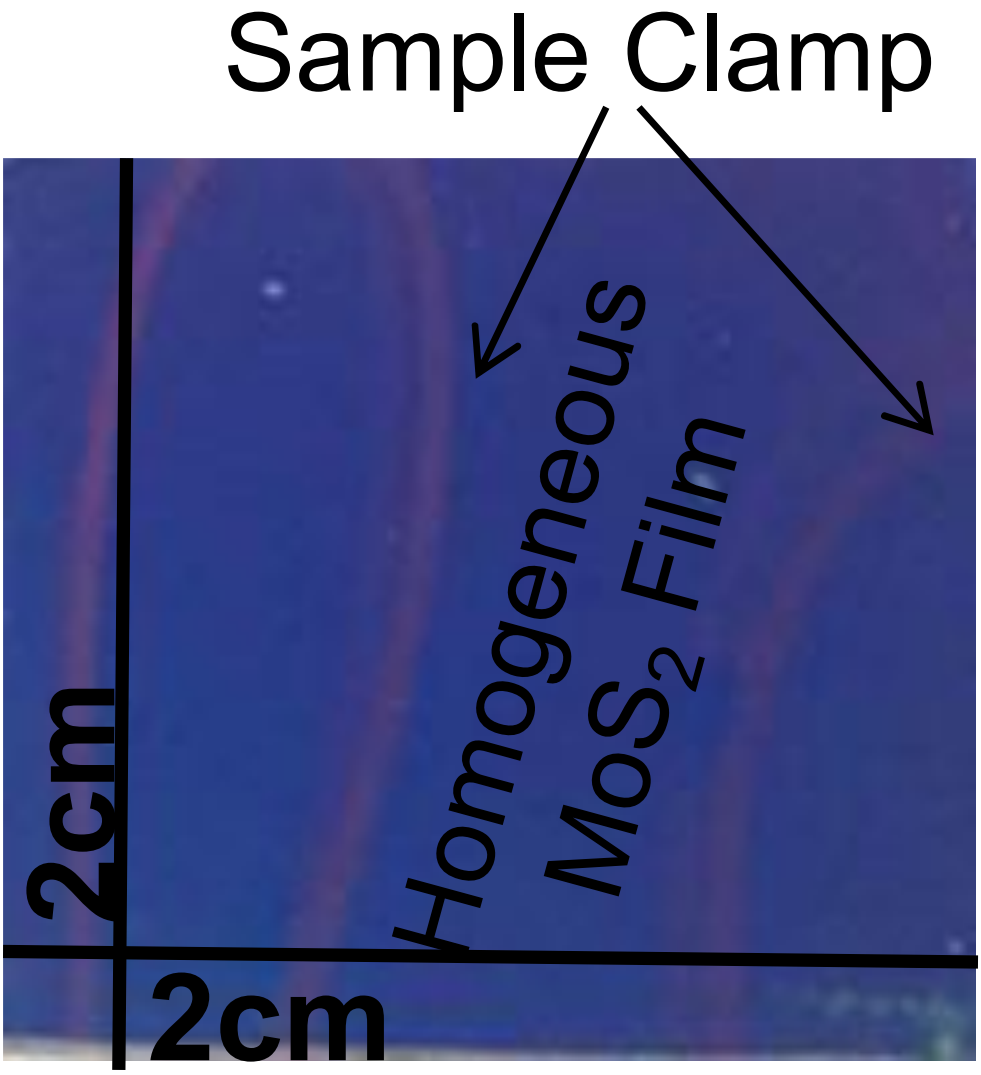

Figure 1.4: This inset shows a 2x2cm^2 piece of wafer with MoS_2 deposited on the surface. The areas shaded purple are areas directly under the molybdenum wire sample holder, as denoted in Figure 1.3.

Further characterization of the films was investigated via optical spectroscopy. Raman and photoluminescence spectra were taken of the films, as shown in Figure 1.5. Raman is an extremely sensitive and powerful tool that probes material via laser to induce molecular vibrations in that material. The location of peaks refers to the energy of that vibration. Photoluminescence is seen when photons are pumped into the material via laser and that material emits light from that excitation of its atoms. For MoS_2, we see the distinctive E^1_{2g} in-plane and A_{1g} out-of-plane vibrational modes at 385cm^{-1} and 405cm^{-1} respectively, as well as the photoluminescence peak at 1.89eV. The Raman separation of 20cm^{-1} is indicative of monolayer MoS_2. The emergence of photoluminescence is only seen at the single layer for most TMDs. Typically, photoluminescence of small island MoS_2 grown with tube furnace CVD is seen at 1.85eV however these films are at 1.89eV. This is likely due to some internal strain effects of a large scaled film versus a small several micron wide island. In the literature, MoS_2 direct bandgap is at 1.90eV, which is shown in the full film case.

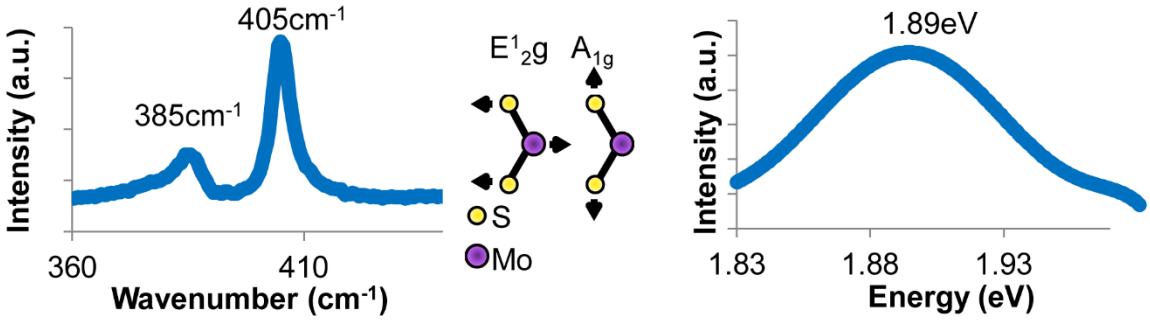

Figure 1.5: Raman and photoluminescence spectra of monolayer MoS_2 created in the CVD vacuum chamber. E^1_{2g} in-plane and A_{1g} out-of-plane vibrational modes at 385cm^{-1} and 405cm^{-1} respectively, as well as the photoluminescence peak at 1.89eV.

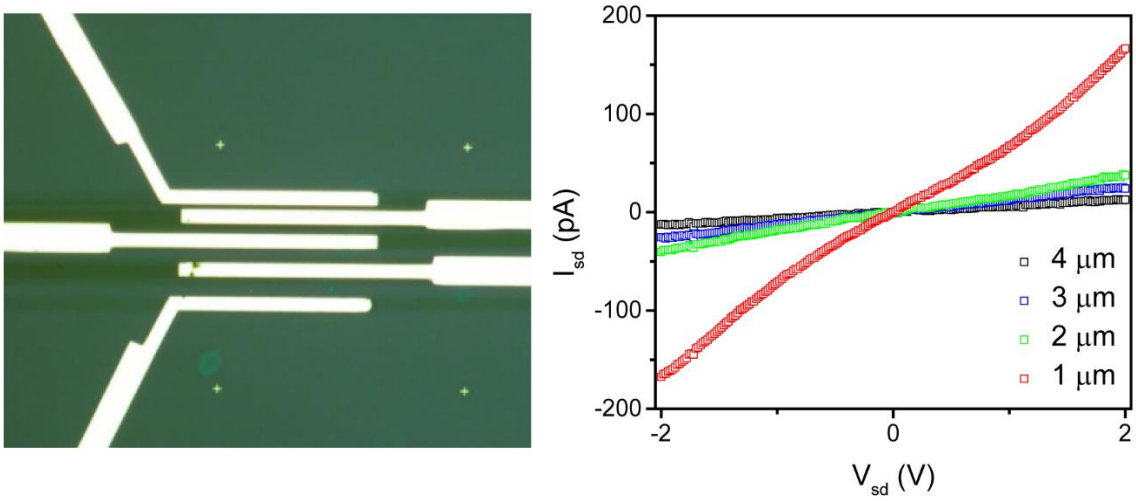

Figure 1.6: A simple FET is fabricated using electron beam lithography (EBL) and deposition of Ti/Au contacts were deposited over the continuous film at various channel lengths from 1-4μm as demonstrated. 2 point *I-V* measurements were taken as shown on the right.

Simple field effect transistors with various channel lengths were drawn via EBL. With varying channel lengths, we did simple 2-point conductance *I-V* measurements and found results in the picoamp regime. This was great progress; however, it shows a long way to go. Although this device was nice for the time, recently a graduate student researcher in our lab, Kortney Almeida, has made great strides on the processes of this chamber which include process times up to 60 minutes which allows her to deposit a high quality, homogenous, and controlled number of layers of MoS_2. Her paper describing growth processes, parameters, optical, and electrical characterizations can be found in ACS Applied Materials & Interfaces.[28]

Other Methods of TMD Synthesis

Other methods were developed such as sulfurization of a metal film which proved moderately effective; however, the crystal size was determined by the homogeneity of Angstrom thick metal on the surface.

There are many other adequate experimental setups to create TMDs, such as molecular beam epitaxy (MBE)[29], e-beam deposition, magnetron sputtering[30], pulsed-laser deposition[31], and atomic layer deposition.[32] However, we find CVD to tailor the needs of our lab for TMD uniformity on the substrate, low impurity, and high film density of the material.

Device Fabrication

Sample Cleaning Procedures

For most cases in fabricating simple field effect transistors, 300nm SiO_2/Si is utilized as a substrate. Sample preparation is the first step for a typical growth process in the Bartels lab is quite simple yet has shown to require gentle and consistent hands. Removal of any large carbon-based residues is achieved by a thorough wash with acetone then isopropyl alcohol (IPA). It is crucial to use enough IPA to completely wash away the acetone to prevent acetone evaporation, leaving a stain on the substrate. Once the substrate is fully rinsed with IPA, deionized water is used again to entirely rid the sample of IPA. This wash with water is key to not only a clean surface, but in practicing good safety for the next step where residual solvent will react with the cleaning solution. The washed substrates are then transferred to clean dry glassware it is ok if the substrates are

damp with water. A piranha solution is created in the new, fully washed substrates glassware with a 3:1 ratio of sulfuric acid and hydrogen peroxide. This cleaning method is excellent at removing any contamination of the growth substrate from metals and carbon-containing materials. A 3-step water rinsing method is then employed to wash the piranha solution away. The rinsed substrates are dried with inert gas (usually N_2 or Ar) and ready for growth or processing.

Electron Beam Lithography

Device fabrication of field effect transistors on 2D materials is a sensitive and crucial step into obtaining reliable electrical data. At the University California, Riverside, the Bartels' Lab utilizes a Zeiss crossbeam SEM with FIB capabilities. At the Army Research Laboratory, the Nanoelectronics Team uses the Vistec EBPG5000+ ES.

The process for device fabrication at UC Riverside has grown and changed a lot with the goal in mind to reduce contamination via reducing process steps or making necessary steps of the process more benign. Specifications of varied processing steps will be mentioned following the general process. The typical process begins after growth of a TMD at UC Riverside has been characterized via Raman spectroscopy and identified to be pristine material. I first deposit a layer of PMMA450 A4 at 4000rpm for 45 seconds on a spin coater which is then cured on a 180°C hotplate for two minutes. This process follows the MicroChem spin curves data sheet. It is repeated once more, if ~400nm PMMA is desired.

The sample is then placed in the SEM crossbeam for patterning a marker layer. Under the SEM microscope, my lab takes great care to make the substrate as visually straight as possible by adjusting the rotation prior to writing markers. The location of the material is obtained, and estimated coordinates are used to move to the targeted area. The finer details of the 2x2mm grid are written with a 20keV beam through a 20μm aperture with a relatively unstable beam current of ~180μA due to the limitations of our cleanroom. The larger alignment pads are written with a 20keV beam through a 60μm aperture with the same beam current. The sample is taken out and developed in a 1:3 Methyl isobutyl ketone (MIBK):IPA solution for ten seconds in still conditions, moved to a 100% IPA bath for ten seconds with a waving motion to stop development, and dried with N_2. The development is checked visually with an optical microscope then recorded.

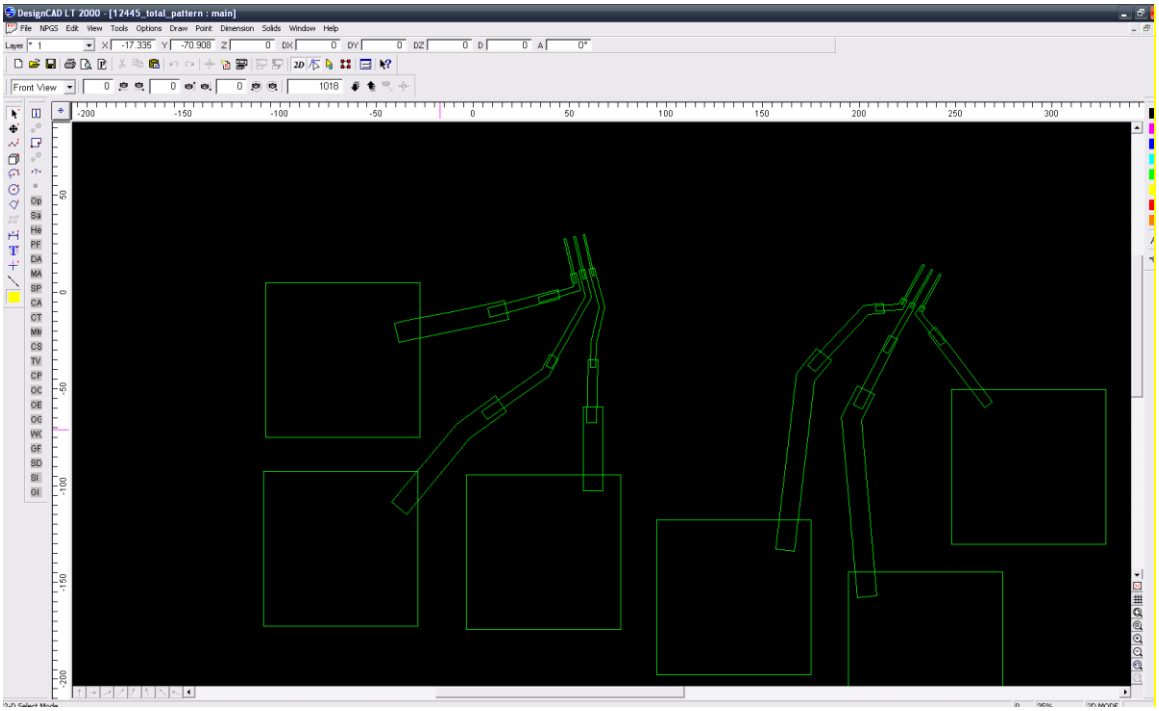

Figure 1.7: Design CAD drawing of two (2) three terminal devices with 1μm distance between contacts.

To metallize the markers, we operated a Temescal electron beam evaporator to deposit 5nm Ti/80nm Au. Titanium is a well-known adhesive metal. Gold is a reflective metal producing the contrast in the SEM to locate markers. A base pressure of ~10^{-6} torr is commonly achieved for metal deposition. Manual control of the system includes a slow ramp in power over a couple minutes and a soak for approximately one minute where the deposition rate is stabilized (1Å/s for Ti, 2 Å/s for Au). The soak's secondary purpose is to remove the top oxide layer of the material by effectively "burning" it away and is performed on the adhesion metal and gold targets. As to PMMA specifications for a liftoff process, we remain well under the minimum 1:2 height ratio of metal deposited to PMMA thickness (in this case, 85/400nm). Liftoff is carried out in a room temperature acetone bath

for 45-60 minutes. After this time period, the sample is sprayed with an acetone spray bottle to assist releasing excess metal from the substrate.

The sample is re-spun right away to protect the surface of the TMD from atmospheric oxidation in the same procedure above with two layers of PMMA. Images are taken of the surrounding areas of the material of interest as well as highly magnified spots of where the material is located. The images are transferred into DesignCAD. DesignCAD is a 2D CAD software that runs specifically on WindowsXP computers and is compatible with the NanoPattern Generation System (NPGS), also exclusively run on WindowsXP, to control the crossbeam SEM. Once the images are fitted into DesignCAD and the devices have been drawn, the file can be exported to NPGS. After designs are imported to the NPGS software, options such as manual alignments, auto movement, and dosages are entered from previous dosage test to create a run file for the crossbeam shown in Figure 1.7.

When the sample is back under the crossbeam, alignment pads are located to adjust the rotation of the sample. Since the markers are made as a grid with equal spacing of 50μm, simple movements from one marker to another are taken adjusting contrast, brightness, beam stigmation, and position along the way. Once at a designated marker according to the images/NPGS, the device patterns are written with a 20keV beam through a 20μm aperture with a beam current of ~180uA and the larger alignment pads are written with a 20keV beam through a 120μm aperture with the same beam current. The sample is taken out and developed in a 1:3 MIBK:IPA solution for ten seconds, moved to an IPA

bath for ten seconds with a waving motion to stop development, then dried with N_2. The development is checked with an optical microscope and logged.

As detailed above, to metallize the devices we use the same e-beam evaporator to deposit 5nm Y/80nm Au. Yttrium is used because it has a low work function[33-35], ~3.2eV depending on the stacking, which is even lower than more common adhesive metals such as Ti (4.3eV), Ni (5.2eV), or even Sc (3.5eV). Gold is used for conductance and its inert surface property under ambient conditions. A base pressure of $\sim 10^{-6}$ torr is usually achieved for metal deposition. Manual control of the system includes a slow ramp in power over a couple minutes and a soak for approximately one minute where the deposition rate is stabilized (1Å/s for Y, 2 Å/s for Au). This time the Yttrium soak is a more crucial step. Since its work function is so low, Yttrium tends to oxidize more quickly than other metals but not as thick of an oxide layer than other metals of a higher work function(e.g. Sc).[36, 37] Liftoff is carried out in a room temperature acetone bath for 45-60 minutes. After this time period, the sample is sprayed with an acetone spray bottle to assist releasing excess metal from the substrate.

Since 2D materials are effectively all surface, contamination at the interface is a major concern. To reduce contamination among devices we have implemented many experimental procedures to effectively reduce processing steps. During each liftoff process, large PMMA residues are shown to remain[38]. Minimizing the number of liftoff steps will effectively decrease the amount of times the surface is exposed to PMMA. To accomplish this, after developing the marker we skip metallization and move directly to imaging the

surrounding area and onward to CAD. Developed ~400nm PMMA has a moderate contrast in the crossbeam, making alignment more difficult, but reduces the number of processing steps.

Due to oxygen in the atmosphere, some TMDs are less stable in ambient conditions than others. Prime example of such TMDs are usually the selenide or telluride based TMDs, such as $MoTe_2$ and WSe_2. The first difference we employ is with the commonly used PMMA A4, which is a polymer dissolved in an oxygen-containing solvent, anisole, $CH_3OC_6H_5$. Although ether compounds are relatively unreactive the use of PMMA C5 (solvent: chlorobenzene, C_6H_5Cl) is necessary which has different spin curves than A4, but similar thicknesses are reached. A second simple way to minimize oxygen at the surface is spinning on PMMA immediately after growth. Lastly, liftoff is performed in an acetone environment. Acetone, C_3H_6O, is an oxygen containing ketone in which we can limit the temperature to room temperature to reduce reactivity and lessen the time we wait for liftoff to occur. In some instances, we have managed liftoff at room temperature in 15 minutes.

As alluded to in the preceding methods to minimize surface interaction, elevated temperatures drive oxidation to occur. There are three areas we control the heated environment our sample is exposed to. According to MicroChem processes, PMMA is optimally cured at 180°C for two minutes for the best resolution. Through experimentation, we have found little difference curing PMMA at 150°C for one minute. During deposition of various metals, it is vital to keep the deposition chamber under 50˚C since depositing certain metals requires longer cleaning cycles which will heat the chamber. Lastly, liftoff

of metalized patterns is done with room temperature acetone for 15 minutes which is usually just enough.

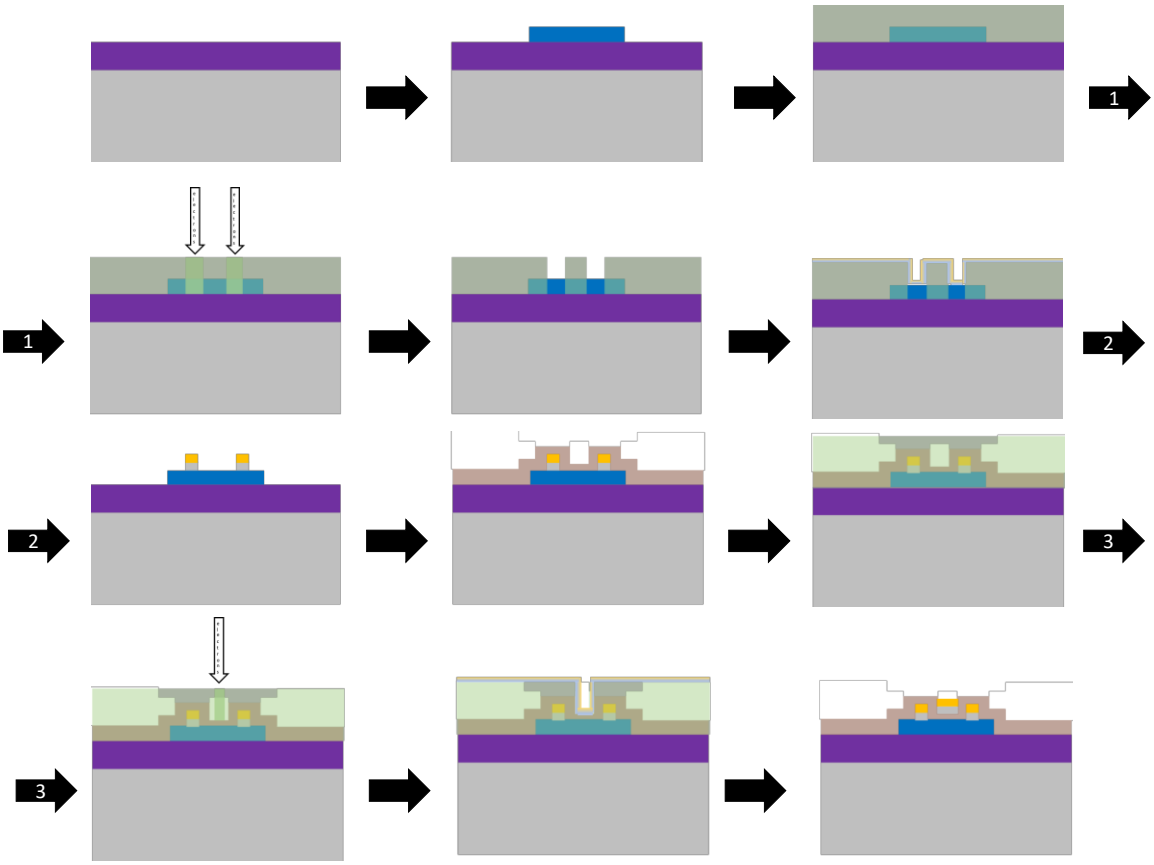

Figure 1.8: Schematic of top gated device fabrication steps at Army Research Lab (ARL).

The process for device fabrication at ARL is fundamentally different than UCR with the main goal in mind to mimic device designs found in CMOS devices. These device structures are directly compared to the CMOS models; however, one must keep in mind in most cases we are dealing with strictly a 2D material while silicon-based CMOS devices are 3D defined. ARL's typical device process follows a series of steps which are visualized in Figure 1.8:

1. Markers
2. Mesa EBL/Etch
3. Ohmic Contact EBL/Deposition
4. ALD Deposition (top gate)
5. Via EBL/Etch (top gate)
6. Ohmic Contact EBL/Deposition (top gate)

The typical ARL process begins after growth of a TMD film. I first spin coat a layer of PMMA950 A4 at 2000rpm for 45 seconds which is then cured on a 180°C hotplate for two minutes. This process is follows the MicroChem spin curves data sheet; it results in a PMMA layer of ~250nm thickness.

The sample is then placed on the Vistec's sample holder for a marker layer write. Before inserting the holder into the EBL tool, we adjust and measure the rotation, height, and center position of the sample to later direct the tool to pattern. Once the holder is loaded, a 2x2cm grid is written with a 100keV beam through a 400um aperture with an extremely stable beam current that can be adjusted from 100pA-100nA. In the case of most processing steps, a 15nA beam is used for optimal speed and accuracy.

The sample is taken out and developed in a 1:3 MIBK:IPA solution for 75 seconds with a waving motion, moved to a 100% IPA bath for ten seconds with a waving motion to stop development, and dried with N_2. The development is checked visually with an optical microscope and recorded.

To metallize the markers, we operate a ChA electron beam evaporator to deposit 15nm Ti/85nm Au. As previously mentioned, titanium is a well-known adhesive metal and gold is a reflective metal producing clear contrast in the SEM to locate markers. A base pressure of ~10^{-6} torr is usually achieved for metal deposition. Automatic control of the system includes two rounds of a slow ramp over about a minute and a soak for about 30 seconds per material. Deposition rates vary for each material; in this system we obtain a rate of ~2Å/s for Ti, 4Å/s for Au.

As to PMMA specifications for a liftoff process, we remain well under the minimum 1:2 height ratio of metal deposited to PMMA thickness (in this case, 100/250nm). Liftoff is carried out in a heated acetone bath (50°C) for 45-60 minutes. After this time period, the sample is sprayed with an acetone spray bottle to assist releasing excess metal from the substrate.

Images are taken of the material of interest and transferred into AutoCAD. AutoCAD is a common 2D/3D CAD software that is updated constantly; the majority of this work utilizes the 2017LT version. Once the images are properly placed in the marker CAD design, we can drag and drop transfer length measurement (TLM) structures, top gated FETs, AC amplifiers, and other test structures. The standard CAD drawing file (.dwg) is converted to a drawing exchange file (.dxf) which can be imported by our primary lithographic software, BEAMER by GeniSys. In BEAMER, the file is imported and separated into layers which are each fractured into simple (rectangular) polygons and healed (re-stitched). The next step is for BEAMER to call upon a Point Spread Function

(PSF), called Tracer. Tracer performs a proximity effect correction calculation based on Monte Carlo simulations of the sample how much the beam doses each polygon for maximum resolution allowable by the beam radius and step size. BEAMER takes all this information and exports to a GUI pattern file (.gpf) usable by the Vistec's GUI based exposure script creator CJOB. Each layer is individually imported into CJOB's mass hierarchical structure (.cjob) where each dosage, stage movement, and beam status are defined. Once every tweak/definition has been entered, we can export each individual layer which can be used by the tool's Linux interface (.job).

Finally, when the sample is back under the EBL tool, beam adjusted and focus checked, the current layer can be written. The mesa layer is written with a PXOR function where a nested rectangle (the channel) is untouched as the pad area is etched away leaving clean SiO_2. After the mesa layer has been defined by EBL, an etch of material is performed with a chlorine-oxygen, anisotropic reactive ion etch on the ULVAC NE550e. The etch consist of 30sccm Cl_2 + 5sccm O_2 for 20 seconds at 200W followed by a subsequent 7 second O_2 etch step to descum the resist top layer.

Subsequent processing steps include spinning another layer of PMMA to define the ohmic contact layer, metallization using the ChA e-beam evaporator (15nm Ti/85nm Au) and lifted off in a warm acetone bath @50°C for one hour. Once microscope images are taken, we can begin 2/4-point probe test measurements.

To fabricated top gate devices, a combination of atomic layer deposition, wet etching vias (trenches), and deposition of contacts is utilized to create a simple source-drain-gate transistor as shown in Figure 1.8.

Chapter 2: Novel TMD Rhenium Disulfide (ReS_2) Growth and Characterization

Rhenium disulfide is a TMD that natively grows in the 1T' distorted octahedral phase, unlike its counterpart TMDs 2H phase. The three phases most common to transition metal dichalcogenides can be seen in Figure 2.1. Atomic size along with this tight lattice helps resist oxidation in 5/6 sulfur sites per rhenium[39], making it more environmental stable even than molybdenum disulfide. According to the literature, the 1T' structure also gives rise to higher mobility due to anisotropy on the b-axis where one can see Re-Re zigzag rows.[12] Peak temperatures during growth only reach 450˚C which makes it a promising material for integration into existing industrial processes. Temperatures are much better than MoS_2 required minimum 650˚C, or tungsten TMDs where temperatures reach upwards of ~900˚C. Unlike typical TMDs where a direct bandgap is only achieved in a monolayer, rhenium disulfide maintains a direct bandgap into the bulk. This is great news for growers as they know how difficult growing a homogenous monolayer film can be. These properties suggest distinctive applications of ReS_2 beyond transparent, flexible devices, such as neuromorphic type devices and non-linear optics which are beyond the scope of this research.

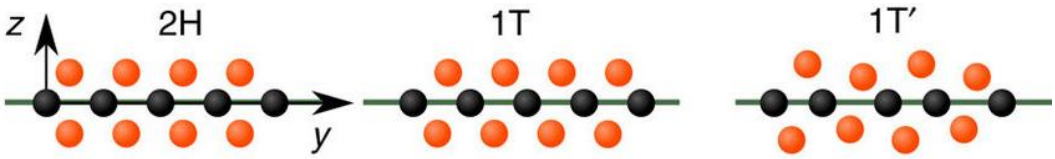

Figure 2.1: Cross-sectional view of the three most common phases for transition metal dichalcogenides.

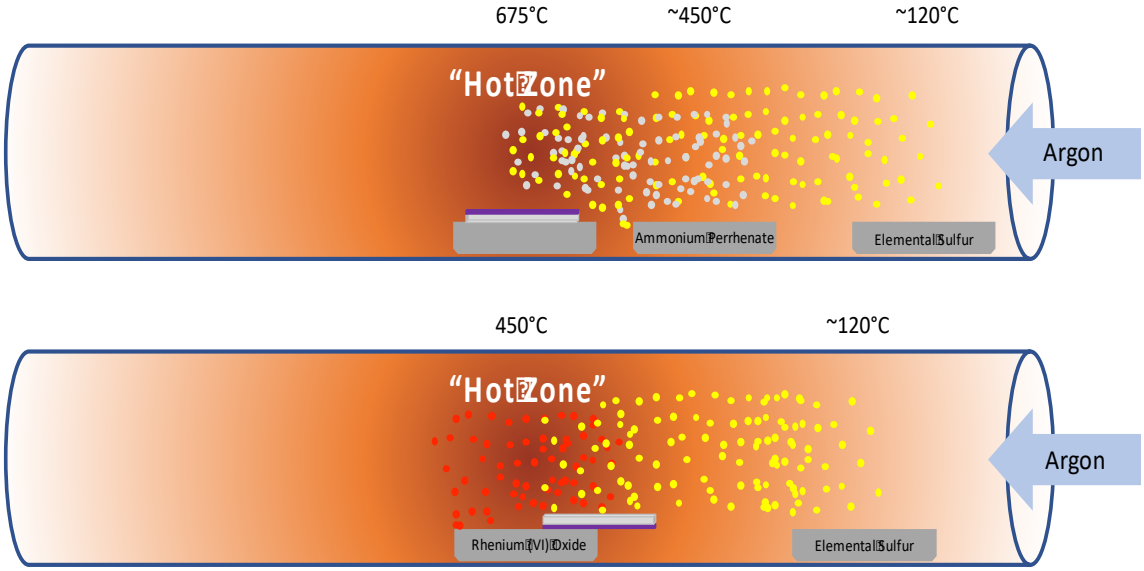

Figure 2.2: Tube furnace schematic for the growth of rhenium disulfide using both ammonium perrhenate and rhenium (VI) oxide as a metal oxide precursor. The primary difference being required temperatures for growth.

CVD growth proceeds in a tube furnace. I have developed methods of synthesizing ReS_2 using two different Re-precursors, ammonium perrhenate and rhenium(VI) oxide, both of which are demonstrated in Figure 2.2. Each precursor provides indistinguishable results. This was done for cost effectiveness, appealing to industrial setting.

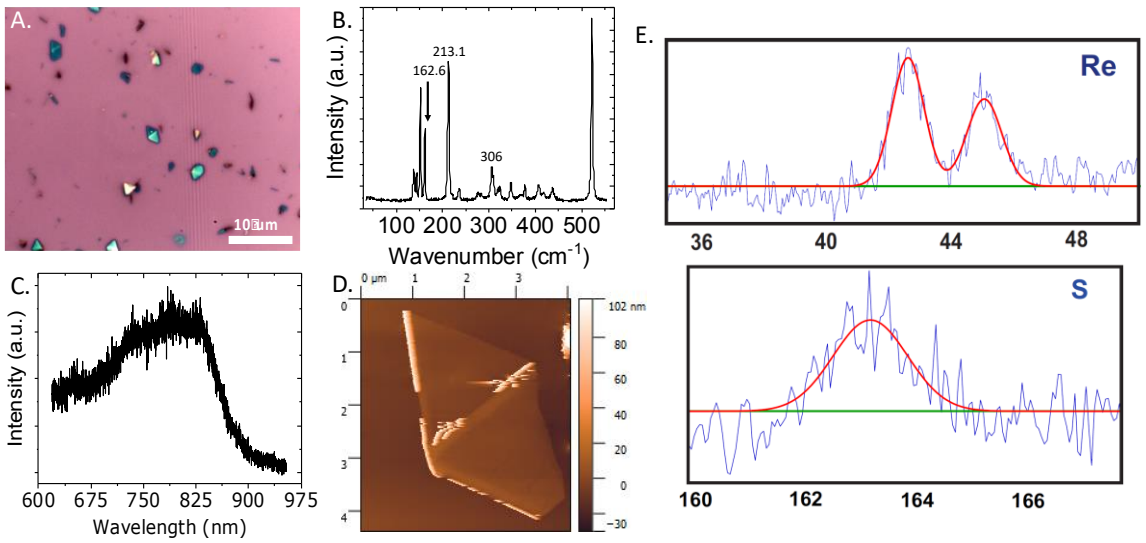

Figure 2.3: a) Optical image of ReS_2 islands. b) ReS_2 Raman spectra of a). c) ReS_2 photoluminescence spectra of a). d) ReS_2 atomic force microscopy of a). e) ReS_2 XPS scans of a).

Optical characterization of this facile CVD grown method aligns closely with literature and expected values, demonstrating adequate material synthesis. Samples were characterized primarily via Raman spectroscopy, using a 532nm laser, and atomic force microscopy (AFM). X-ray photoelectron spectroscopy was performed to characterize the elemental bonding of the CVD grown rhenium disulfide. The rhenium cores $4f_{7/2}$ and $4f_{5/2}$ are located at 43 and 45eV, respectively, while a sulfur core $2p_{3/2}$ is positioned at 163eV. The location of these peaks strongly supports the indication of metal-sulfide bonds. We note that each peak was shifted by ~2eV than the values reported in the literature[40], subtraction of our copper standard accounts for this discrepancy. Rhenium disulfide has a DFT calculated direct band gap at 1.35eV for bulk material and 1.65eV for monolayer and shifts depending on thickness.[12] Photoluminescence measurements were taken in each sample; however, results are inconsistent. Wu *et al.* mentions that photoluminescence may

not be discernable if the grains of the crystal are too small.[41] Photoluminescence in CVD grown ReS_2 is rarely present but may be explained by these reasons. To confirm the thickness of few-layer ReS_2 material, atomic force microscopy was performed. Each monolayer of ReS_2 has been measured to be ~0.7nm with an astonishing 0.6nm interlayer distance.[12] In Figure 2.3d, the island was measured to be 7.3nm, corresponding to six monolayers of ReS_2.

Raman signatures for few-layer to bulk ReS_2 are reported ~162 cm^{-1}, ~213 cm^{-1}, and ~306 cm^{-1}, indicating E_{2g}, A_{1g}, and E_{1g}-like vibrational modes, respectively. Many additional Raman modes arise between 100-400 cm^{-1} due to the distorted 1T' structure causing symmetry splitting.[40] One important aspect of the 306 cm^{-1} E_{1g}-like peak is that it can easily be overshadowed by a silicon zone boundary peak[42] ~300 cm^{-1} in thin samples.

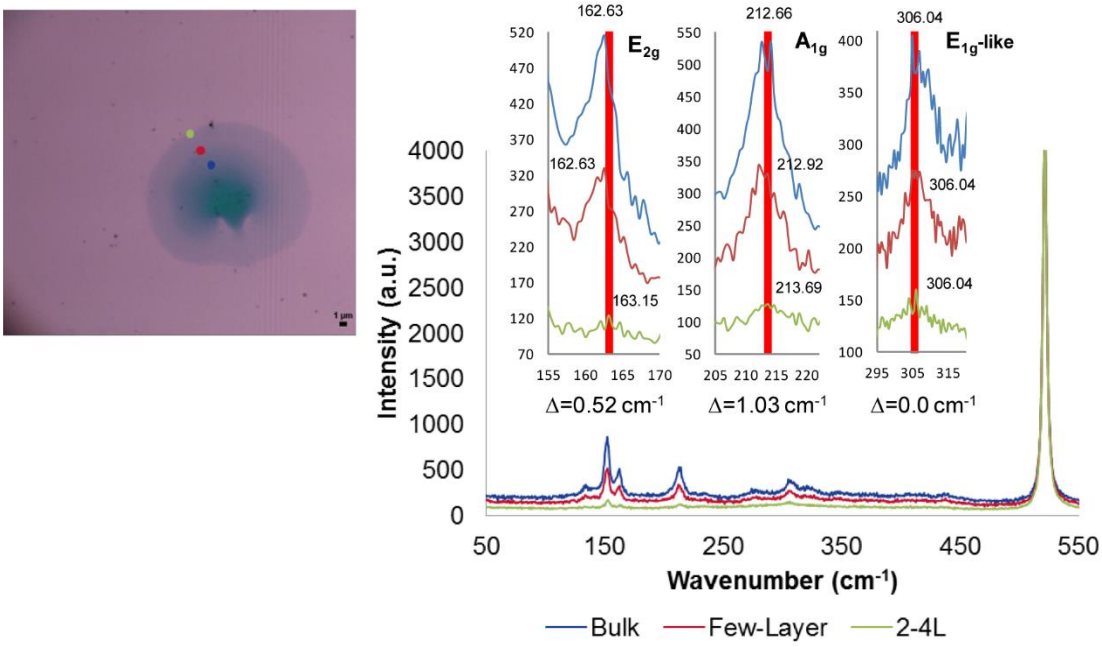

Figure 2.4: ReS_2 Raman study of varying film thickness.

To observe this more closely, I found a film region with varying optical thickness and took Raman measurements at each point. Green as the "2-4 layer," red as the "few-layer," and blue as the "bulk". Calibrating to the silicon peak, we can see a small yet clear red shift of the E_{2g} and A_{1g} peaks, which has been described in the literature. The E_{1g}-like mode remains constant regardless of number of layers which can provide us with a nice standard to normalize our peaks in the future.

ReS_2 Raman Study

The unit cell of 1T' rhenium disulfide contains 12 atoms which correlates to 36 total vibrational modes, 18 of these modes being Raman active.[43] Raman spectroscopy is a sensitive, powerful characterization technique that uses a laser to probe phonon interactions in a material system, such as vibrational modes. Thermal properties and structural transitions of a material may be probed by varying the temperature and taking Raman spectra in small temperature steps of 5K.

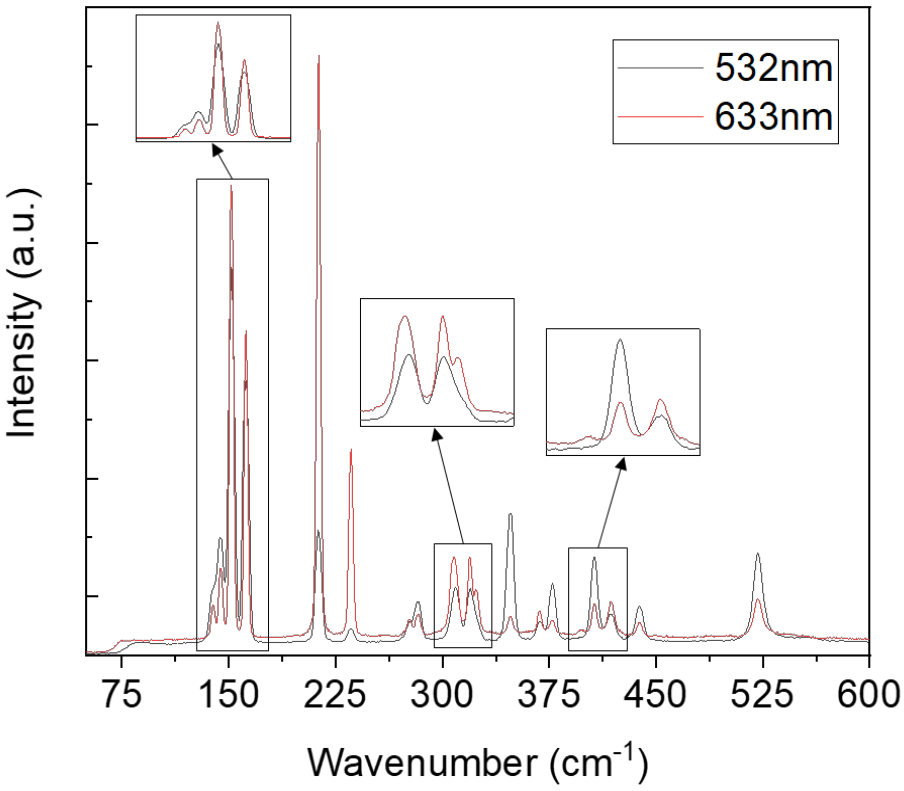

Figure 2.5: Bulk rhenium disulfide Raman spectra at 532nm (black, green laser) and 633nm (red, red laser).

In this experiment, we use Raman spectroscopy and explored a range of temperatures from 77K-480K to extract the thermal conductivity of bulk, exfoliated ReS_2. Different wavelengths of light interact differently with various materials systems. In the spectrum of Figure 2.5, lasing wavelengths 532nm (green) is compared with 633nm (red). Using the same laser power, we observed more pronounced splitting of the Raman active modes using the 633nm laser, suggesting ReS_2 to be in resonance at this wavelength. Most of the peaks are affected by the change in wavelength, a few are shown in detail, notably the emergence of the peak located at $348cm^{-1}$.

Each vibration is an in-plane A_g mode; however, significant out-of-plane components are shown in eigenvectors. These modes are renamed by Feng et al. to specify contributing out-of-plane modes and listed in the table below. As there are 18 active Raman modes[44], only one of each primary vibration is shown on the right and are very well representative of other trends. After a Raman spectrum was taken, each peak was fit to a Lorentz curve where the peak position was calculated. Plotting peak position vs. temperature shows us two separate regimes. The slope from 300K-480K can be explained completely by the first order temperature coefficient explained by the Grüneisen model where ω_o is the 0K harmonic frequency.

$$\omega(T) = \omega_o + \chi T$$

The general slope extracted from 77K-300K could suggest second and third order temperature coefficients. The bump between 150K-280K is unexplained by typical phonon

interactions and may indicate structural phase change (1T' to Td) or opto-electronic change, such as formation of charge density waves.

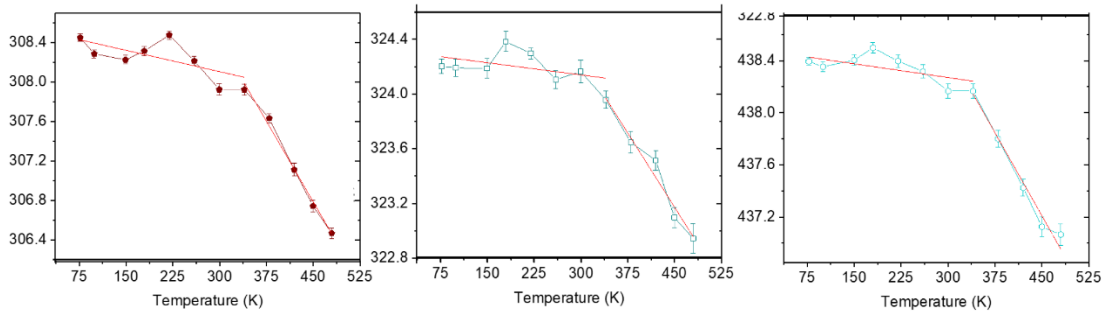

Figure 2.6: ReS_2 Raman shift vs Temperature.

ReS_2 Electrical Characterization

To test transport characteristics, we used a 2-point arrangement and plotted *I-V* curves. We expected FET performance in the ReS_2 devices, which could be tested by measuring transport characteristics as a function of a voltage applied to the substrate as a back gate (V_g) underneath 300nm of silicon dioxide with a dielectric constant ε_r=~3.9.[45] In Figures 2.7 and 2.8, we were able to plot electrical characteristics sweeping source-drain V_{sd}=±4V for different back gate voltages between V_g=±50V. Increasing V_g resulted in higher I_{sd}. This characteristic is indicative of n-type material, where Figures 3.7 shows more clearly the n-type behavior at a constant V_{sd}=+4V fit with an exponential function. As higher V_g were used, a small amount of leakage current was measured; however, this

current was two orders of magnitude lower than the current carried through the material and can be subtracted easily.

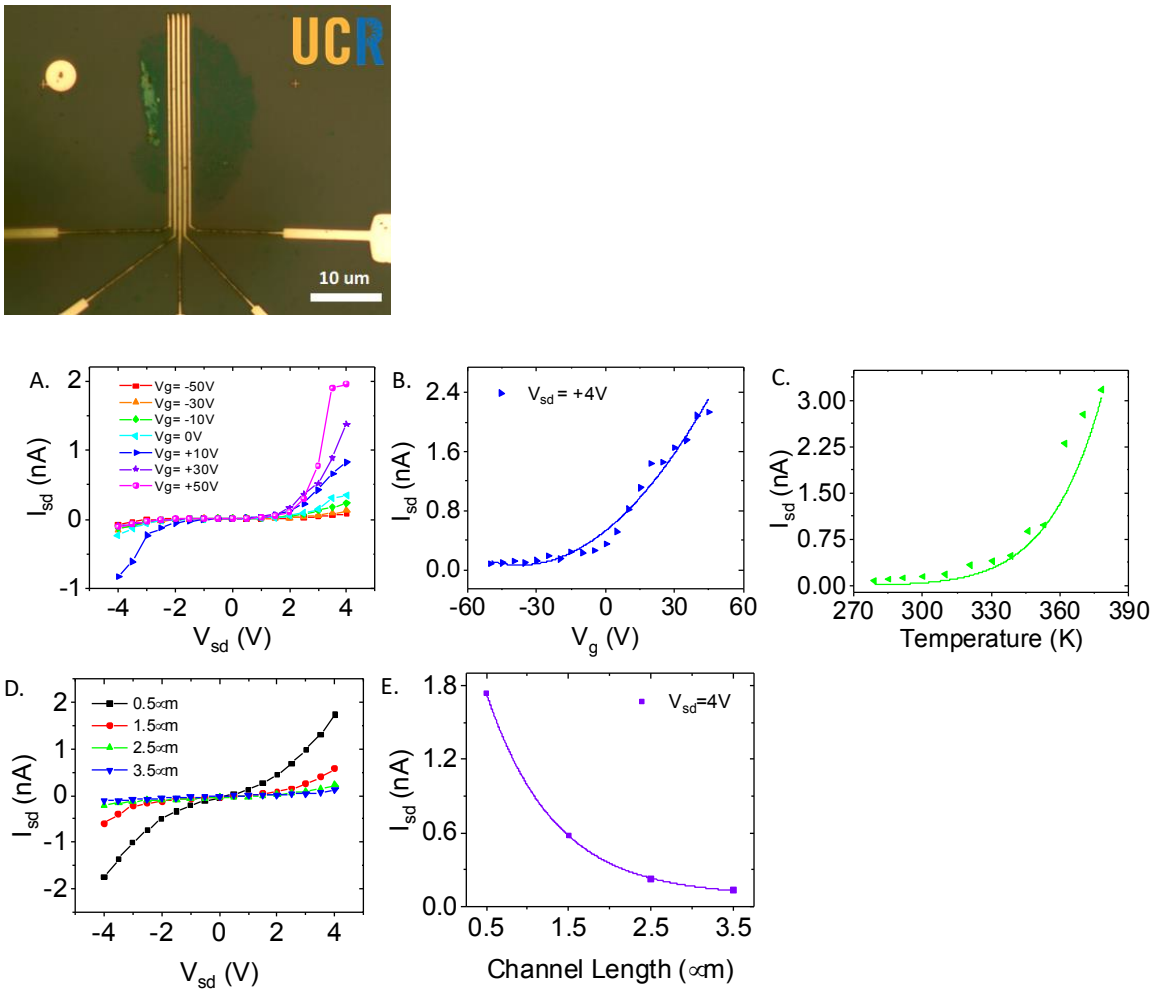

Figure 2.7: Electrical *I-V* characteristics of ReS_2 fabricated at UCR.

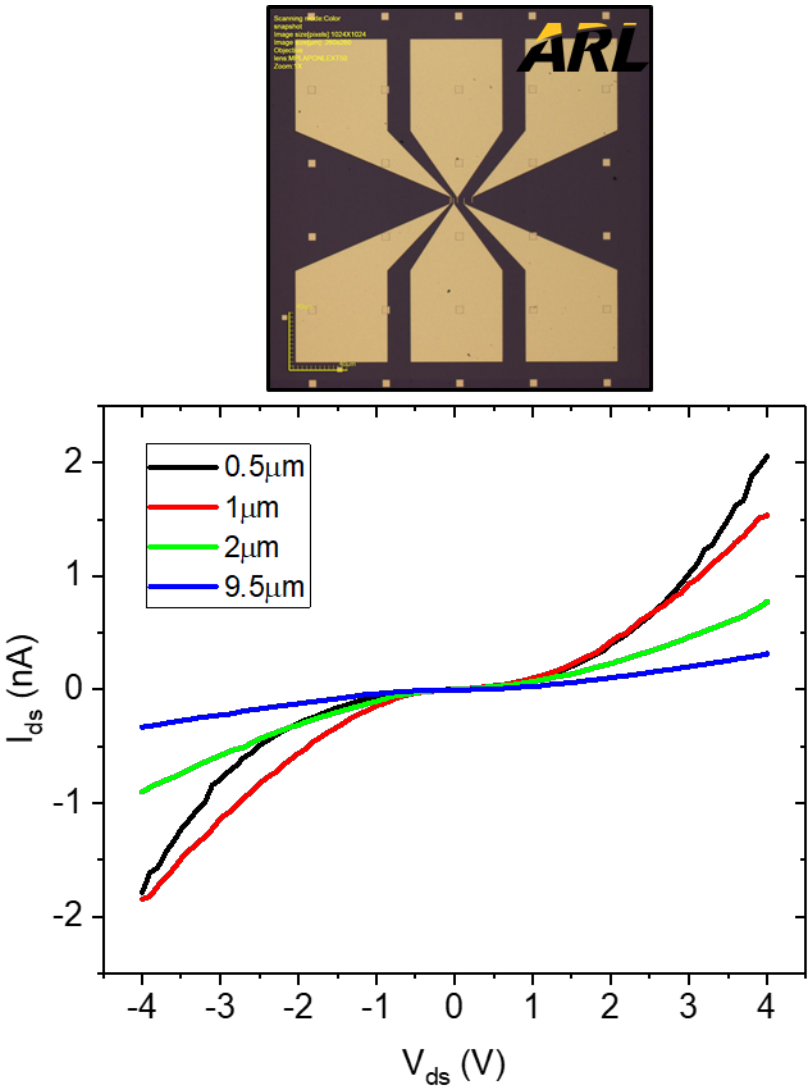

Figure 2.8: Electrical *I-V* characteristics of ReS_2 fabricated at ARL.

Device performance can be varied in several means other than the effect of a gate. Figures 2.7 shows the temperature dependence of a 0.5μm channel device: as the temperature increases, the output current also increases. Figures 2.7d also indicates how the width of the channel influences the current yield. The influence of temperature can be fit to an Arrhenius plot, suggesting a first order increase in the chemical potential of the

material as a function of temperature. The channel-length-dependence yields an exponentially fit, making down-scaling of future ReS_2 electronics even more appealing.

The next step in electrical characterization is to determine the field-effect mobility of our CVD grown ReS_2. This is calculated using the following equation:

$$\mu_{FE} = \frac{\Delta I_{SD}}{\Delta V_G}\left(\frac{W}{L} C_{ox} V_{SD}\right)^{-1}$$

where W and L are the width and length of the material inside the device channel, and C_{ox} corresponds to the capacitance of the dielectric, SiO_2.[46]

To measure the electrical characteristics, I fabricated metal contacts by electron beam lithography at UCR and ARL. At UCR, I utilized Sc/Au contacts and at ARL I used Ni/Au contacts. In the *I-V* measurements below, we can see the conductance of the material is quite low. At ARL we found slightly better channel conductance, likely due to improved metal deposition. However, transfer length calculation shows the contact resistance and sheet resistance to be in the low giga-ohms per micron regime, which is extremely high for 2D FETs, suggesting high Schottky barriers.

We see a similar trend on the UCR device when gating, where the Schottky effect is so overwhelming it is tough to extract reliable material properties from the data. Despite these barriers we can see a slight gate effect that shows us the CVD grown ReS_2 is, in fact, *n*-type.[47]

Motivation

Looking at the lattice parameters and structures of various 2D and 3D semiconductors, we find notice a close match between MoS_2 with the (0001) plane of the 3D semiconductor gallium nitride. Both TMDs and GaN have a hexagonal crystal structure and the lattice parameter (*a*) that are similar of one another, suggesting epitaxial growth of TMDs on gallium nitride may be possible. Gallium nitride and most single-layer transition metal dichalcogenides lattice parameters have been modeled with temperature by various researchers.[48-52] Since TMDs are grown at temperatures ~900-1100K, lattice match at growth temperatures may be more important than at room temperatures. Table 3.1 lists lattice parameters at room temperature and TMD growth temperature. The sulfides match most closely at room temperature, both with about ~1% lattice mismatch. The lattice match is even better for MoS_2 at growth temperatures; unfortunately, no structural data for tungsten TMDs was found for elevated temperatures.[53]

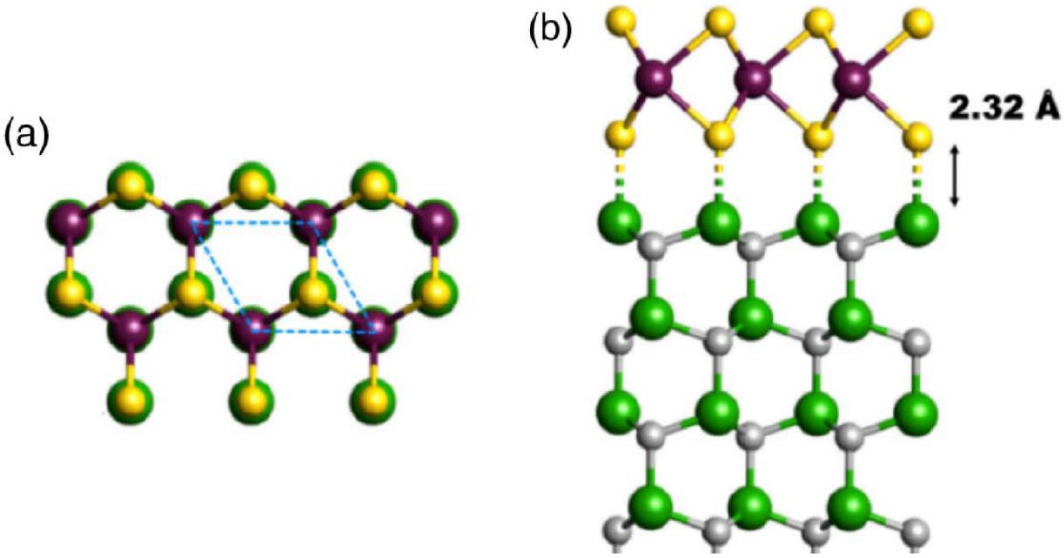

Figure 3.1: MoS2 on GaN lattice matching. a) top-down view, b) cross-section view.[54]

Strain may be an effect to consider but is beyond the scope of this project.[55, 56] MoS_2 is one of the most intensively studied 2D semiconducting materials since it has been found to be the most chemically stable and has desirable optical and electrical properties, including an energy bandgap between 1.3-2.2eV depending on layer count.[57, 58] Gallium nitride is used for high speed, high power devices and is find application in radar, guidance systems, and wireless communication. Since MoS_2 is the closest to GaN and there are established methods at the Army Research Lab and in the Bartels lab to grow *n*-layers, we find MoS_2 to be the best target for 2D/3D heterostructures.

Materials	a (Å) (@650˚C)	% difference from GaN (@650˚C)	a (Å) (@RT)	% difference from GaN (@25˚C)
GaN	3.197	0.0%	3.187	0.0%
MoS_2	3.181	0.5%	3.161	0.9%
$MoSe_2$	3.309	3.5%	3.299	3.5%
WS_2	-	-	3.153	1.1%
WSe_2	-	-	3.286	3.1%

Table 3.1: Lattice parameters (*a*) for gallium nitride and various transition metal dichalcogenides.

In previous studies, a transferred layer of *p*-MoS_2 was placed onto a *n*-GaN substrate and showed this 2D/3D heterostructure can work as a bipolar semiconductor diode.[59] Ruzmetov *et. al*. showed an integrated Au/2D/3D heterojunction on both *n*-doped and *p*-doped GaN with epitaxially deposited Au nanodots on single crystal MoS_2 flakes

deposited via powder CVD on a high-quality GaN surface. The nanostructure of these dots was examined and tested for electrical conductance.[60] The comparison between *I-V*s of bare GaN, MoS_2/GaN, and Au/MoS_2/GaN via conductive AFM (CAFM) was made. The charge transport was dominated in each case by the tip/GaN interface, implying a single-layer of MoS_2 is electronically semi-transparent.[53]

Growing the 3D layer of GaN on top of the 2D layer of MoS_2 is vital to the development of a vertical 3D/2D/3D heterostructure system, such as a heterojunction bipolar transistor (HBT), where the emitter/collector layers of GaN sandwich the base layer of MoS_2. Successful growth of GaN via MBE on top of CVD-grown, single-layer MoS_2 has already been shown by Tangi *et al.*[61] MoS_2/GaN heterojunctions have also shown to carry large current densities by fabrication of Esaki tunnel diodes.[62]

The Army Research Lab proposes a 3D-2D-3D device following a HBT structure with an n/n^+-GaN collector, few-layer *p*-MoS_2 acting as a base, and *n*-GaN emitter. Figure 3.2 shows a crossectional view of the proposed device.

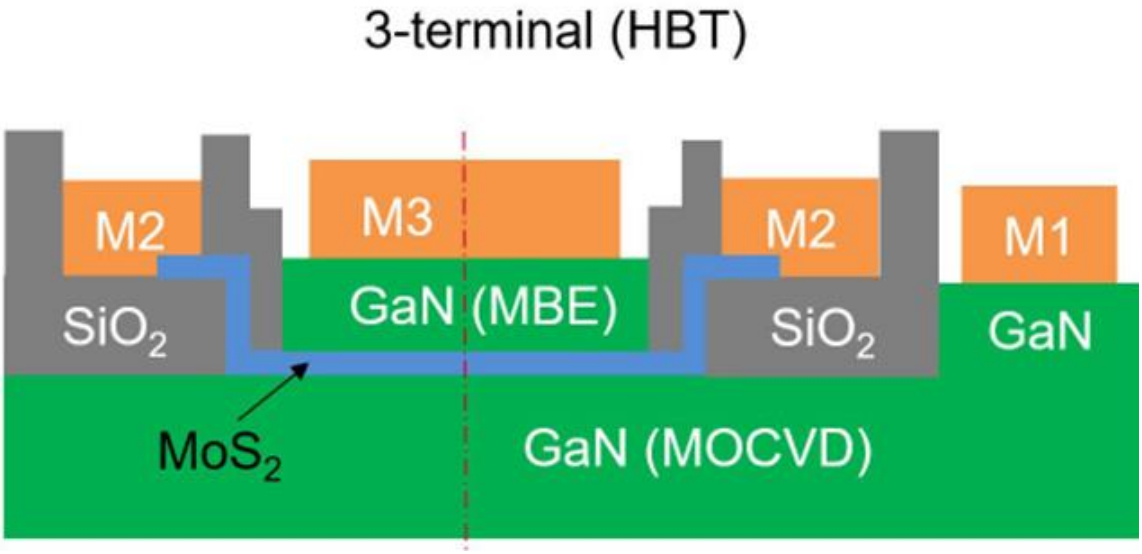

Figure 3.2: Crossectional view of purposed 3-terminal *n-p-n* & *p-n-p* heterojuntion bipolar transitors with GaN as the emitter/collector and MoS_2 as the base.

Two-terminal Transistor

To achieve this device structure we begin with a 4" wafer of 1μm highly doped GaN (n/n^+- via Si or p- via Mg) deposited using MBE by NTT-AT (Japan) atop 500μm c-plane SSP sapphire wafer. The wafer is coated with a protective layer of photoresist (AZ5214) that was soft baked at 110°C for 2 minutes. Once the wafer has been diced into 10x10mm pieces, the photoresist is washed away with acetone. A layer of ~200nm PMMA A4 is spun

at 2000rpm and baked at 180°C. Electron beam lithography (EBL) (Vistec EBPG5000+ES) is used to create a marker layer defined in AutoCAD 2018LT. The pattern is developed in a 1:3 MIBK/IPA solution for 75 seconds. Blanket titanium metal is deposited at room temperature via electron beam evaporation (ChA) at a base pressure of 10^{-6} torr. A liftoff process in a hot acetone bath at 50°C for 1 hour is used to remove the excess metal. Titanium is used over other metals for two processing purposes. First, titanium metal has high contrast in the SEM/EBL to our GaN surface, which is essential to the marker layer. Secondly, titanium creates a thick oxide layer effectively making the metal inert for the later growth process.

At the Army Research Lab, a rigorous cleaning procedure is then performed. Substrate pieces are placed in a PRS3000 (Transcene) bath at 80°C for 15 minutes followed by a second room temperature PRS3000 bath which is sonicated for 5 minutes. Each piece is rinsed in a water bath followed by a 5 minute room temperature baths in acetone then IPA. AFM confirms the cleanliness of the GaN surface showing little to no photoresist residue. Figure 3.3 shows a clear image of the GaN teracene with a surface roughness of 0.12nm for a 5x5μm image.

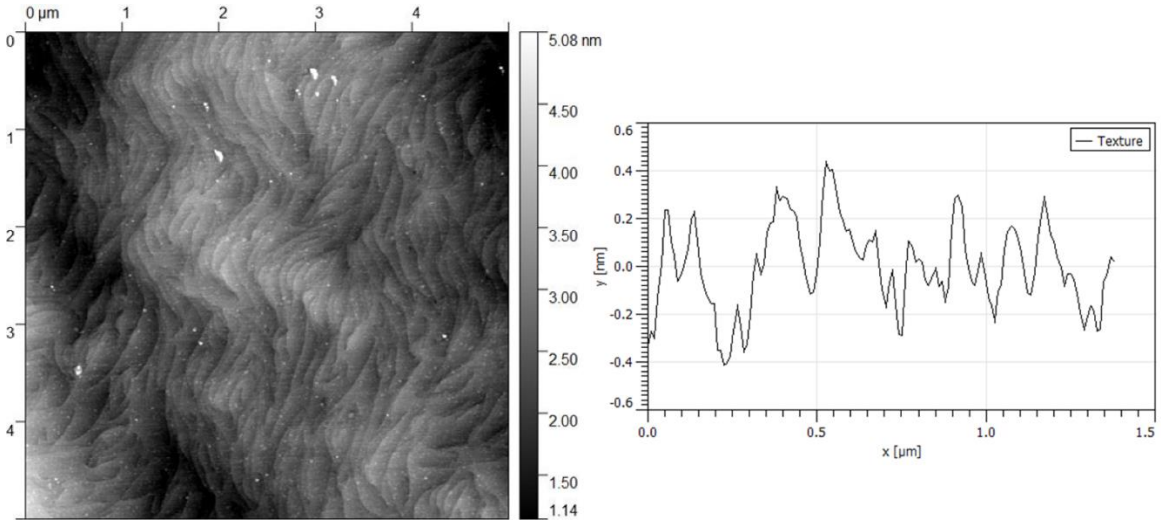

Figure 3.3: Atomic force microscopy image of the terraence of GaN. Resist residue can be seen by white dots. The shallow terrace of GaN, however, is clearly visable.

Once the substrates are cleaned, a plasma enhanced chemical vapor deposition (PECVD) process is used to deposit 100nm SiO_2 at 250°C (Plasma Therm 790+) with a deposition rate ~50nm/minute. We use 100nm thickness for sufficient electrical separation from the MoS_2/GaN terminals and refraction of that thickness is useful for tools like Raman spectroscopy. To create SiO_2 in the PECVD a flow rate of 300 sccm SiH_4He, 1300 sccm N_2O, and 1300 sccm N_2 are injected ino the chamber with a plasma source bias of 300W. Once deposited and cooled, a layer of ~200nm PMMA A4 is spun at 2000rpm and baked at 180°C. EBL is used to define the SiO_2 mesa area (yellow), developed the same way as above, then etched using a wet buffered oxide etch (6:1 HF/NH_4F) with an etch rate of ~70nm/min for 2 minutes and rinsed in water multiple times to halt the etch. The PMMA is removed with a hot acetone bath at 50°C for 1 hour. AFM confirms the height of the SiO_2 ring structure, as well as the roughness of the SiO_2 and GaN surfaces.

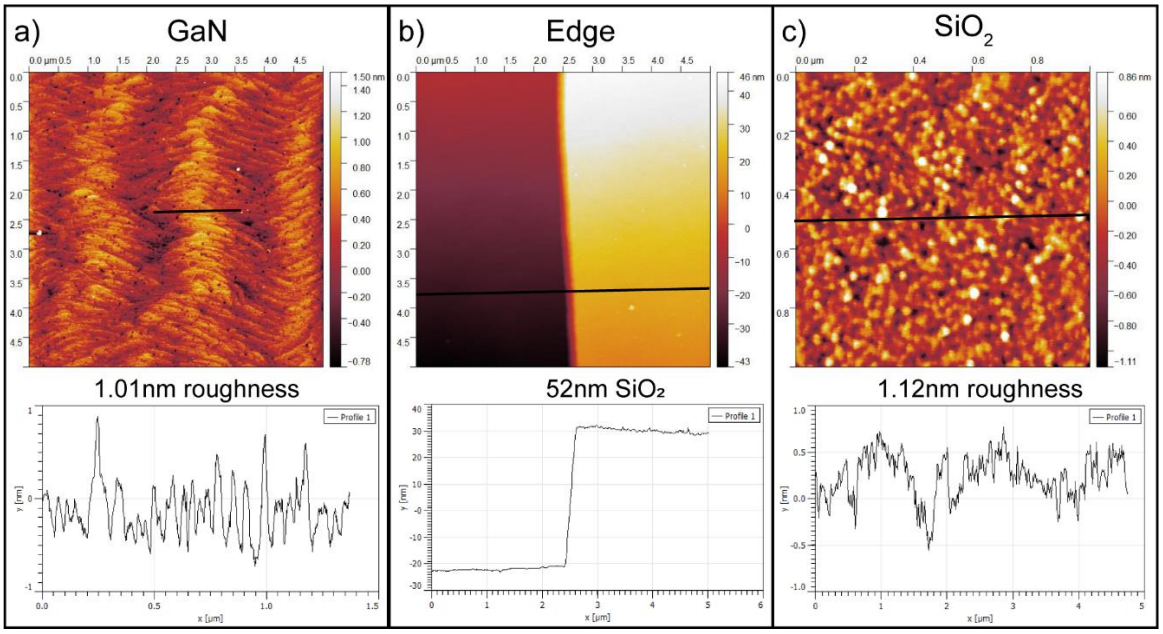

Figure 3.4: AFM images and surface roughness characerization of PECVD SiO_2 on GaN substrate. a) Surface of GaN after SiO_2 deposition and etching. b) Edge of SiO_2 ring on GaN. c) Surface of PECVD SiO_2 ring.

To assure a clean surface for MoS_2 deposition, the sample is boiled in Remover PG at 80°C for 3 hours and inspected with an optical microscope. Multiple rounds of Remover PG may be used, if the surface is not clean. To confirm the quality of the surface, atomic force microscopy (AFM) is used to see the terreance of the GaN substrate and to confirm the absence of resist residues. (Figure 3.4)

The samples are then sent to Kehao Zhang in Joshua Robinson's group at the Pennslyvania State University for MoS_2 depostion via metal organic chemical vapor depsotion (MOCVD). The MOCVD growth process at Penn State University includes both such elements in their reactants. For this growth, Zhang utilizes molybdenum hexacarbonyl

[$Mo(CO)_6$] and diethyl sulfide [$C_4H_{10}S$] as well as a potassium chloride [KCl] as a growth kinetics assistant in increase grain size of synthesised MoS_2.[63, 64]

When the samples are returned, a layer of PMMA is deposited by the same method mentioned above. EBL is again used to define the mesa of the MoS_2 which is then etched using a reactive ion etch (RIE) (Ulvac NE550e) using 30sccm Cl_2 + 5sccm O_2 followed by a subsequent O_2 etch step to descum the resist top layer. In Chipara et. al., this chlorine etch is developed to etch MoS_2 in a more clean manner than an O_2 etch alone or a CH_4+O_2 chemistry which effects SiO_2. This is critical to device realiability.[65]

The PMMA is then washed away with acetone and another layer of PMMA is deposited for the contact layer. EBL defines the contact layer and a blanket 15nmTi/85nmAu metal layer is deposited via ebeam evaporation. In Mazzoni et. al. (in prep, ARL), they show the Ti/Au contact to MoS_2 to have the least contact resistance when performing transfer line measurements. A liftoff process of heated acetone removed excess metal from the pattern.

Considering the contact to the GaN substrate, ideally, metal-semiconductor contacts are Ohmic contacts; however, due to Schottkey barriers/p-n junctions, most contact to semiconductors are not truly Ohmic. Using the reisistance for a regular 3D semiconductor, such as GaN, we can reduce the Ohmic resistance (R) off the contact by increasing the area:

$$R = \frac{L\rho}{Wt}$$

To make near-Ohmic contact to GaN, a drop of photoresist (AZ5245) is cured overnight and used as a mask for the device area. The same chlorine RIE is used on the outside of the device area to etch away and clean the GaN surface. Once the photoresist is removed, an aluminum hard mask is created to deposit large-area Ni/Au contacts on the cornor of the device substrate. Ni/Au contacts have been shown to have low contact resistance to GaN.[66]

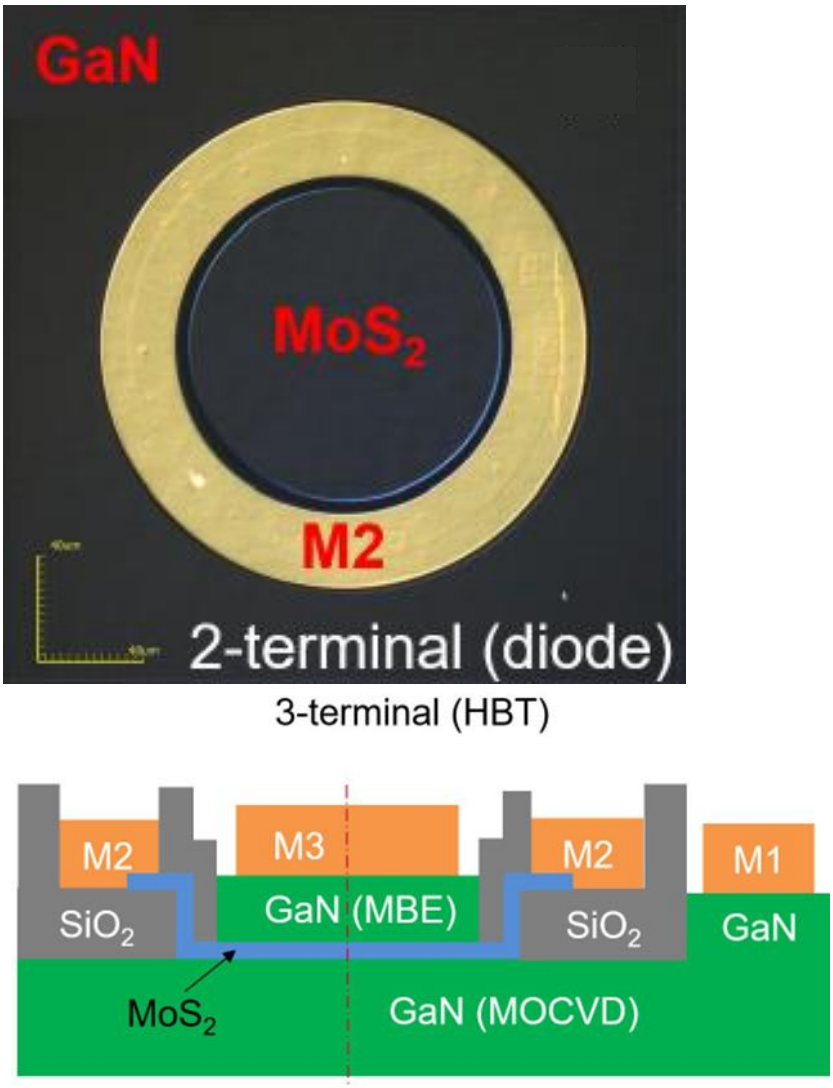

Figure 3.5: 4L *p*-type MoS_2/*n*/n^+-type GaN 2-terminal device in comparison to the desired device goal.

The *n*-type GaN/*p*-type MoS_2 device can be tested as is, however, the *p*-type GaN/MoS_2 is annealed in an argon environment at 650°C for 20 minutes to reactivate the Mg dopant in the GaN lattice.[67]

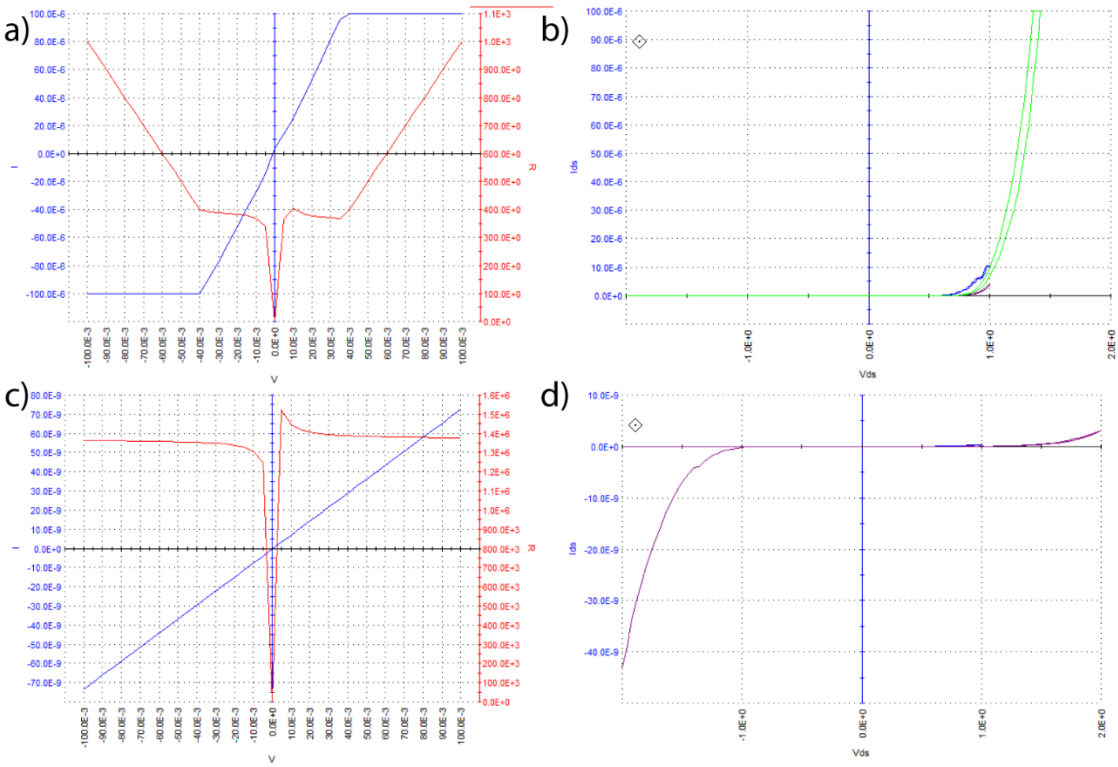

Figure 3.6: a) n/n^+-type GaN conductance *I-V* curve (blue) and *R-V* (red). Resistance >400Ω. b) 4L *p*-type $MoS_2/n/n^+$-type GaN 2-terminal device shows sharp rectification. c) *p*-type GaN conductance *I-V* curve (blue) and *R-V* (red). Resistance ~1-2MΩ after anneal in N_2. d) 4L *n*-type MoS_2/*p*-type GaN 2-terminal device shows rectification.

In Figure 3.6, we see *I-V* curves of both the pn junction and the np junction 2-terminal device. The n/n^+-type GaN resistance is low (400Ω) allowing more current in the pn junction device. Even after an anneal at 650˚C in N_2 atmosphere, we were unable to reactivate the surface for the *p*-type GaN whose resistance ended up multiple orders of manitude larger than the n/n^+-type GaN. Regardless, both devices perform decently with

the 4L *p*-type MoS_2/*n*/n^+-type GaN 2-terminal device showing sharp rectification on par with what we were expecting. Furthur testing showed some resistance anomolies which were then explored via TEM.

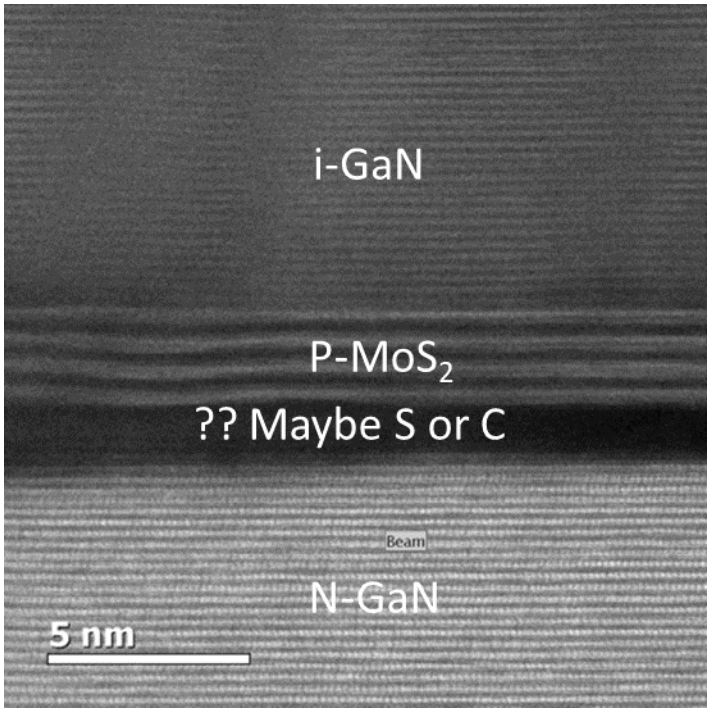

Figure 3.7: Crossectional TEM of the full desired heterostrcuture growth stack. *p*-type MoS_2 was grown via MOCVD at Penn State. *i*-GaN grown epitaxially on top via MBE at ARL. An unknown layer anomoly spotted, leading to future study.

Interfacial Surface Science

Gallium Nitride Cleaning Study

Cross-sectional transmission electron microscopy (TEM) imaging shows an unknown, amphorous layer of material at the interface in Figure 3.7. A rather disturbing finding was measurements from Raman spectroscopy and electron diffraction spectroscopy in TEM disagree on the chemical makeup of this layer. Raman Spectroscopy at the Army

Research Laboratory (ARL) suggest an amorphous layer of carbon between the MoS_2 and n/n^+GaN substrate. Electron diffraction spectroscopy (EDS) in the TEM at the National Institute of Standards and Technology (NIST) measurements show it to be a layer of amorphous sulfur.

As shown above in Figure 3.3, a rigorous cleaning of GaN substrates is decent enough to AFM (atomic force microscopy) the native terrance of the surface.

Examining the MOCVD growth process at Penn State University includes both such elements in their reactants. As described, Zhang utilizes molybdenum hexacarbonyl [$Mo(CO)_6$] and diethyl sulfide [$C_4H_{10}S$] as well as a potassium chloride [KCl]. The potassium choloride is meant to assist the kinetics of the growth. In this way, KCl is heated to 600°C where it melts to create a vapor phase. When in contact with the substrate, the potassium is thought to create a passivication layer on the GaN surface that assists with the kinetics of creating larger grains of MoS_2 and a more homogenous layer of MoS_2. With the use of sodium cholride [NaCl], Zhang and others have shown a 20x grain size increase and thr resistant of bilayer crystal growth. In this study, Zhang uses potassium KCl in the same method in his experiments. It seems a differing mechanism than predicted is occuring, causing that amphorous layer of material.

At the University of California, Riverside, we can grow MoS_2 in a different, yet similar method as described in Chapter 1: High-Vacuum Filament Growth mastered by Kortney Almeida while I was at ARL.[28] In this method, elemental molybdenum wire and H_2S gas is used within a high vacuum chamber which would greatly decrease potential

contaminates as well as lower the chances of unwanted elements adsorping to the surface. With a base pressure of $1x10^{-7}$ torr or better, the unit Langmuir can be used to describe this advantage. Langmuir is defined by multiplying time of exposure to gas pressure, where 1L would suggest one molecule/atom hitting the surface in one second at 10^{-6} torr. With this, we can estimate that at the base pressure of the chamber each surface atom is hit by a gas molecule every other second. This is far better than at atmospheric pressure where approximately 10^{10} gas atoms/molecules hit the GaN surface atoms every second. By focusing on cleaning and maintaining a clean GaN surface, we hypothesize a contaiminate-free interface between MoS_2/GaN.

First, to focus on the cleaning steps which we can analysis via x-ray photelectron spectroscopy (XPS) in the Bartels' Lab. We do an XPS analysis of the surface before these cleans and name them "as received" substrates. At ARL, we clean the surface with at least 2 hours in 80°C Remover PG, a 10 min bath in PRS3000 at 80°C, a new bath of PRS3000 sonicated at room temperture for 5 min, then cleaned in a piranha solution for 5 min. We have shown via AFM above that this cleans the surfaces fairly decently, however, a different cleaning study has been done to improve the interface between III-V and TMD.

In the XPS, we scan for multiple elements for a variety of reasons. A gallium 3d scan will show the characteristic gallium peak. The literature shows this peak at ~18.7eV. If we scan out to past 0eV, although virtually impossible, we find the valence band edge of the material at positive binding energies which we can improve based on surface cleanliness. A nitrogen scan helps us determine the Ga:N ratio of the surface of the

material. We expect the Ga:N ratio to be over 1 since nitrogen is the limited reagent in the growth process of GaN from lack of simple nitrogen precusors. When MoS_2 is deposited, we expect the nitrogen scan to exhibit a secondary peak which would be the attraction between MoS_2 and GaN. A scan of oxygen will show us how much of the surface is oxidized to Ga_2O_3, a common surface layer material on gallium nitride due to the high reactivity of oxygen in the atmosphere and lower crystal energy of the oxide over the pure material. A carbon scan can quantify the amount of advantitious carbon adsorped on the surface, in addition to carbon unintentially incorporated into the films. A carbon and oxygen scan can also be analyzed to determine the amount of CO adsorped to the surface from a ultra high vacuum environment. Confirmation of carbon and oxygen being reduced can be determined by the ratios of CO:C and CO:Oxides. Removing oxygen and carbon from the surface of gallium nitride has proven difficult by many research groups.[68-76]

With a variety of cleaning methods and systematic studying of the surface of GaN with XPS, we aim to make the surface as pristine as possible before the growth of MoS_2 in high vacuum. First is to explore the effect of solvents ARL uses for their studies with a subsequent piranaha clean. Then, I explored wet etch chemistries for oxides following the piranaha clean. Lastly, I focused on making the surface pristine with sputtering and annealing, which lead into a deeper study of sputtering effects.

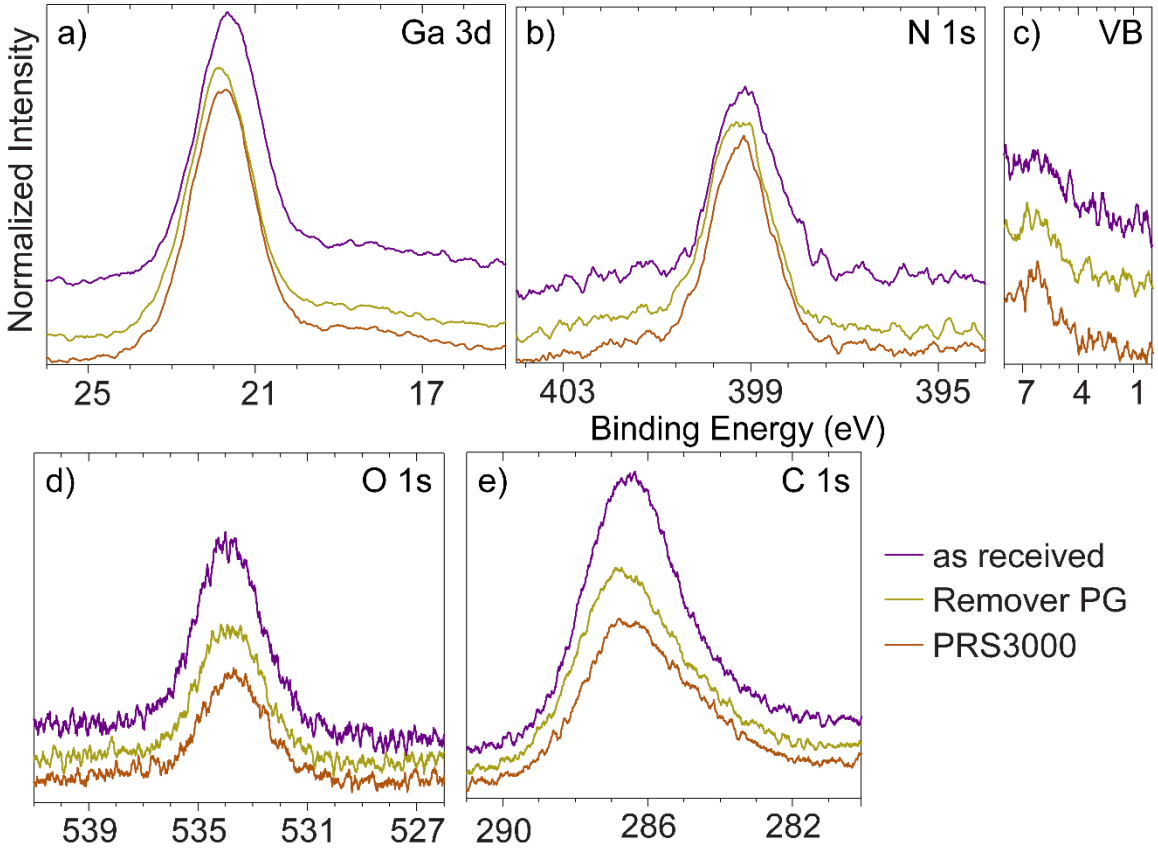

Figure 3.8: Solvent cleaning study of *n*-type GaN showing results of Remover PG and PRS30000 versus an as received sample from the manufacturer. Normalized to the Ga3d peak: a) Ga3d, b) N1s, c) valence band edge, d) O1s, e) C1s.

Each graph is normalized to its respective Ga3d peak to see ratios of gallium on the surface to other species studied. Figure 3.8a shows these ratios intensity versus binding energy. In gallium 3d the ratio is 1:1, while in nitrogen 1s the ratio is 13:20, suggesting the surface to be gallium rich with nitrogen spanding 65% of the surface. Using this nomencalture, adventitious carbon is a known contaminate amoungst spectroscopist. The theory being anything exposed to atmophere will effectively deposit a thin layer of carbon across the sample. Carbon covers most of the surface of our GaN substrate as expected.

The goal being to reduce the amount of carbon that has accumlated on the surface over time as well as any contaminates introduced during processing/dicing.

Exploring the effect of solvents used before the cross-sectional TEM are Remover PG and PRS3000. The solvent baths were for 2 hours at 80°C, rinsed with deionized water, then quickly inserted into the XPS to avoid exposure time to atmosphere. Focusing on Figure 3.8e since that is where we see the most change. Remover PG and PRS3000 both have a common ingrident n-methyl-2-pyrrolidone (NMP) which is a powerful organic solvent, however, each has its own patented formula. Remover PG reduced the Ga:C ratio ~30%, but the PRS3000 goes down considerably about 45%. In conjunction with future cleans, PRS3000 is proven to be a powerful tool to clean our substrates.

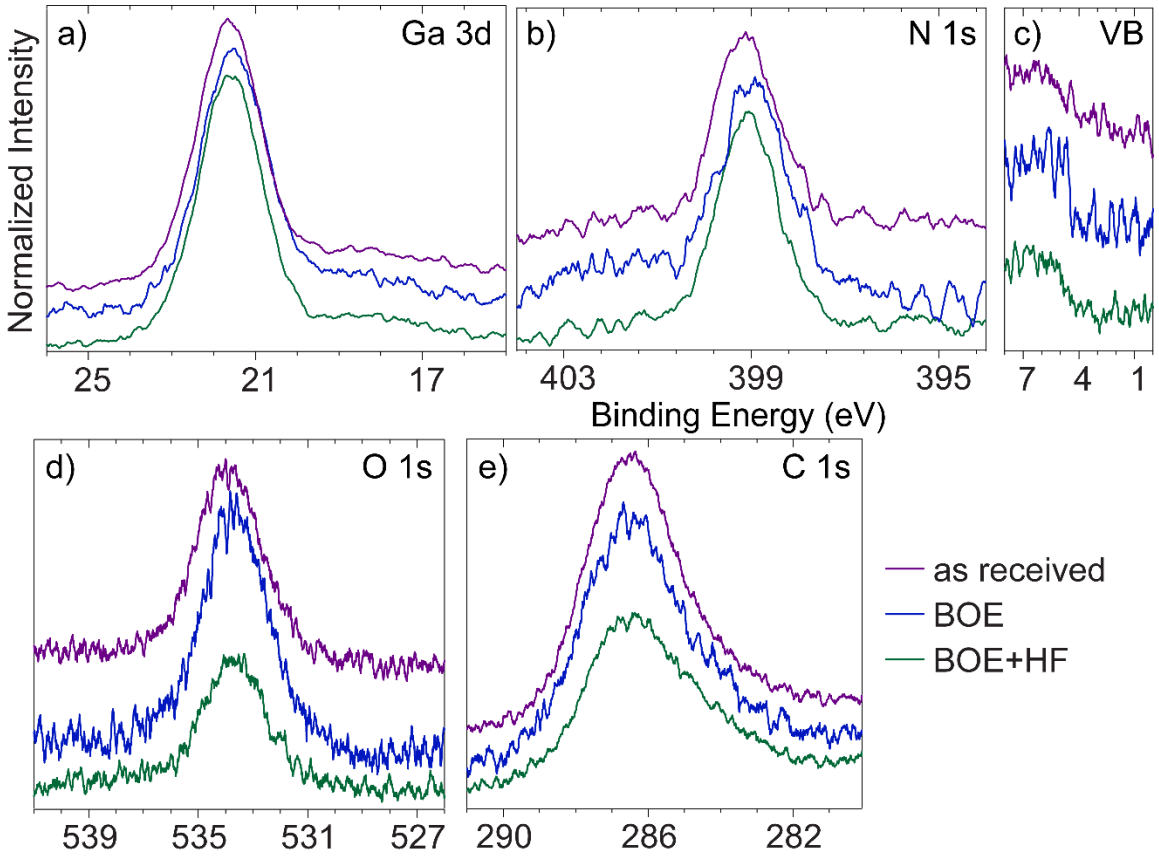

Figure 3.9: Oxide wet etching study of *n*-type GaN showing results of BOE and HF versus an as received sample from the manufacturer. Normalized to the Ga3d peak: a) Ga3d, b) N1s, c) valence band edge, d) O1s, e) C1s.

Next was the assessment of oxide wet etch chemistries. On the sample as received we see oxygen outnumbers nitrogen on the surface of the gallium nitride. This is likely Ga_2O_3 which, like most metals, oxidizes on the surface with the oxygen in the atmosphere. Buffered Oxide Etch (BOE) [1:6 HF:NH_4F] is a well known oxide etchant and HF can potentially flourinate the surface ensuing BOE[77]. At this time we also explored using distilled water bubbled with hydrogen gas to maintain the surface and decrease the amount of dissolved oxygen.[78] Each addition of a chemical was analyzed by XPS. The procedure

was a 5 minute bath in piranaha, 5 minute bath in BOE, 5 minute bath in HF, rinse and transfer in hydrogen bubbled distilled water, then quickly dried and inserted into the XPS for a vacuum environment.

In Figure 3.9d, we first look at the effect of only BOE. One can see an increase of oxygen at the surface of GaN when only BOE cleaning is performed, however, a drastic decrease with both BOE+HF baths. Considering the surface chemistries at play, we can assume BOE is effectively etching oxide from the surface of the GaN substrate. The problem why we see more oxygen soon after is likely due to exposure to the oxygen in the atmosphere during transfer and may even be oxidizing in the H_2 bubbled water during transfer from the cleanroom to the XPS. Although speed and caution is taken when loading the sample into the XPS, overall less than a minute process, is detrimental to the surface and reoxidize exposed gallium atoms.

Following the BOE clean with an HF bath is our proposed method to fill the vacanies on the gallium nitride surface, at least long enough to transfer into a more stable vacuum enviroment. With just an added 5 minute bath of HF, we can see a nice reduction to the oxygen 1s peak by about 50%. As alluded during the BOE bath, it seems HF is doing a great job filling the surface vacanies after the oxide wet etch with BOE. This is critical in protecting the GaN surface until we can potentially replace the flouride ions with nitrogen in the next step. We also see an improvement in the clarity of the valence band edge of GaN which is important but the greatest difference coming from the future anneal.

After reducing carbon contaiminantion and surface oxides, we explore making the surface pristine by potentially rehomogenizing the surface before growth of MoS_2. Nitridation of GaN surface has been studied by various methods in previous studies.[79-85] Common methods include annealing and making use of a direct/remote nitrogen plasma or ammonia gas enviroment. There are a few methods we can go about annealing GaN in the Bartels' Lab. With an abdunce of tube furnaces, we could anneal a substrate in a tube furnace flowing either N_2 or NH_3.

Nitrogen is a common gas we flow in tube furnaces, however, reaching temperatures to activate a surface reaction is difficult, requiring temperatures over 1000˚C. Ammonia is a much more reactive gas and would utilize lower temperatures between 650-800˚C. The primary concern here would be safety. Most CVD setups are graduate student built, which is great in most regards, however, since mostly inert gases are used to facilitate a small chemical reaction, we do not have the proper engineering controls to flow a more corosive gas like NH_3. In both methods of using a tube furnace for annealing, the problem remains how to keep the surface pristine for MoS_2 film growth during transfer from system to system.

To reduce atmospheric exposure, we can utilize ports on the MoS_2 growth chamber to either create a remote N_2 plasma or flow more corrosive gas since we do have proper engineering controls for vacuum chambers. A leak valve would use very little of the gas at all in comparison to atmospheric or even low pressure options. N_2 plasma, even if remote,

can potentially damage the surface with energetic particles. Since we can accuratly dose gases in the vacuum growth system, we opted for annealing in a ammonia atmospshere.

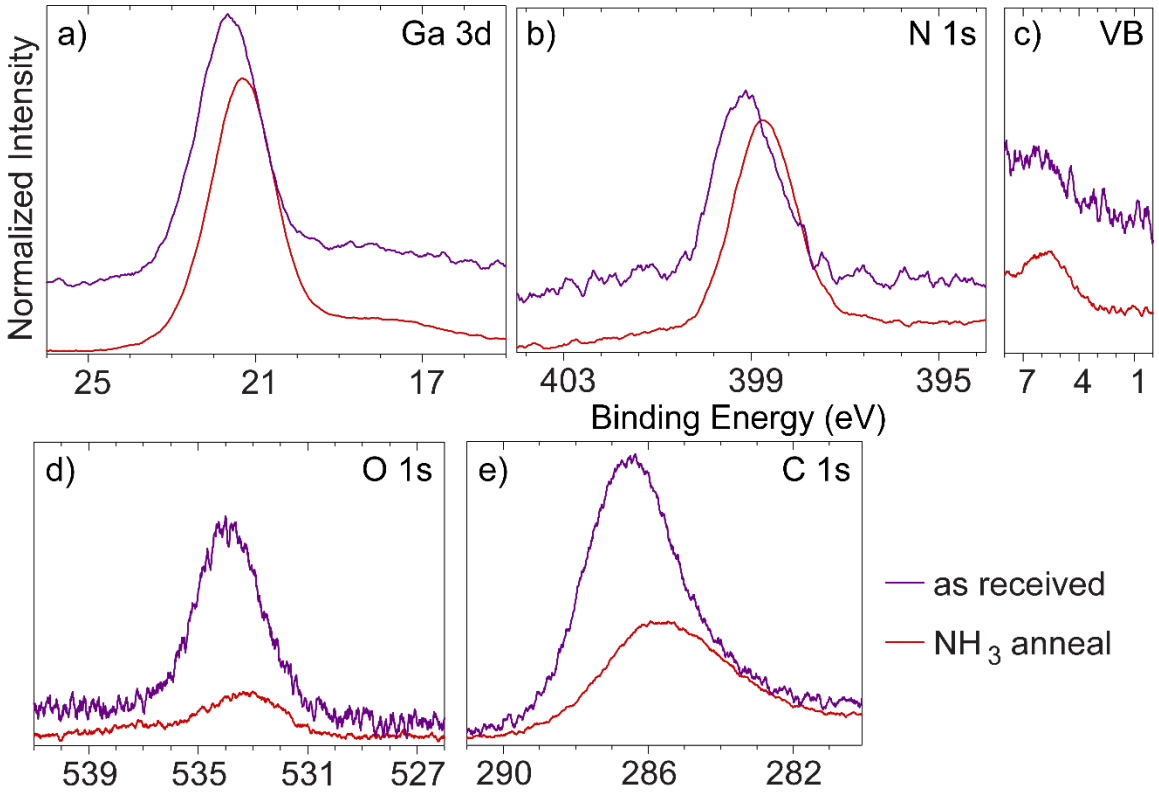

Figure 3.10: Annealing cleaning study of *n*-type GaN showing results of an anneal at 750˚C in NH_3 environment ($4x10^{-4}$ torr) versus a received sample from the manufacturer. Normalized to the Ga3d peak: a) Ga3d, b) N1s, c) valence band edge, d) O1s, e) C1s.

Starting with a base pressure of $1x10^{-7}$ torr, we start by ramping our hotplate to the desired annealing temperature. One the hotplate has degassed a bit by reaching 70˚C, we leak ammonia gas to a pressure of $4x10^{-4}$ torr. Continuing to ramp the hotplate, we monitor the pressure to keep a consistant flow of ammonia gas. Once at maximum annealing temperature (750˚C in the case of Figure 3.10) is reached, we hold the temperature for 15 minutes. During ramp down of the hotplate, we continue to flow ammonia until the system

is below 200˚C, which we then pump out excess ammonia returning to high vacuum at $1x10^{-6}$ torr since the chamber is warm. For XPS analysis we still must transfer the sample through atmopshere from the MoS_2 growth chamber to the XPS.

In Figure 3.10, we most notably see a significant shift in all the scans, however, most ratios of elements stay similar from the combination of previous cleans with much less noise. Taking a closer look at the valence band edge of the ammonia annealed sample, by fitting the band edge we obtain a value of 3.0eV. In the as received sample we obtain a value of 3.92eV. Here it is important to remember to take our internal standard into consideration to make an accurate analysis of the data, which is 0.85eV. Gallium nitride has a bandgap of 3.5eV.[86, 87] Since the material is *n*-doped, we would expect to see the fermi level closer to the conduction band of the material. Taking the internal reference into account, the as received sample's fermi energy is sitting 0.43eV below the conduction band. This would infer the material is degeneratly *n*-doped. Taking the same measurement with the sample had been treated with wet cleans and the ammonia anneal in vacuum, we see the shift of the fermi energy to be 1.35eV below the conduction band, which is still indicative of *n*-type material. Since all graphs are in reference to the fermi level of the detector, we can assume this shift is due to the unpinning of of the fermi level.

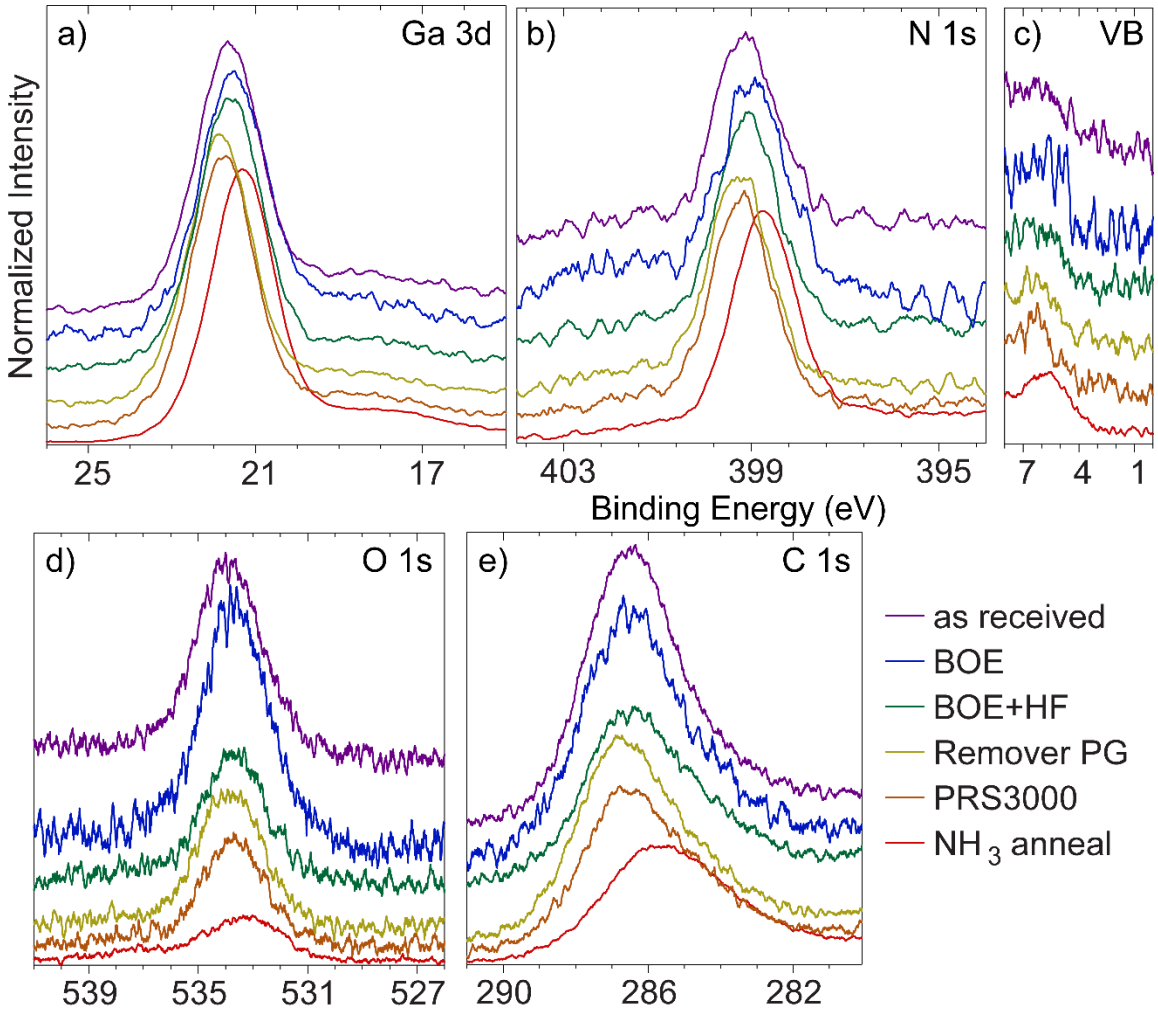

Figure 3.11: Total cleaning study of *n*-type GaN showing results of the combination of solvents, wet oxide etch chemistry, and a NH_3 anneal. Normalized to the Ga3d peak: a) Ga3d, b) N1s, c) valence band edge, d) O1s, e) C1s.

Figure 3.11 shows the combination of all the cleaning treatments we employed at the University of California, Riverside. With the complete treatment we found most effective being a 5 minute bath in PRS-3000 to remove large carbon-based residues, 5 minute piranaha clean to clean solvents and smaller carbon-based residues, 5 minute BOE clean to remove oxides on the surface, 5 min HF soak to flourinate the vaccanies, transfer

to a vacuum system by way of H_2 bubbled water, dried with N_2 and straight into a high vacuum chamber for NH_3 anneal at 750˚C. This treatment method was able to unpin the fermi level, effectively showing the pristine surface of GaN we were able to reveal.

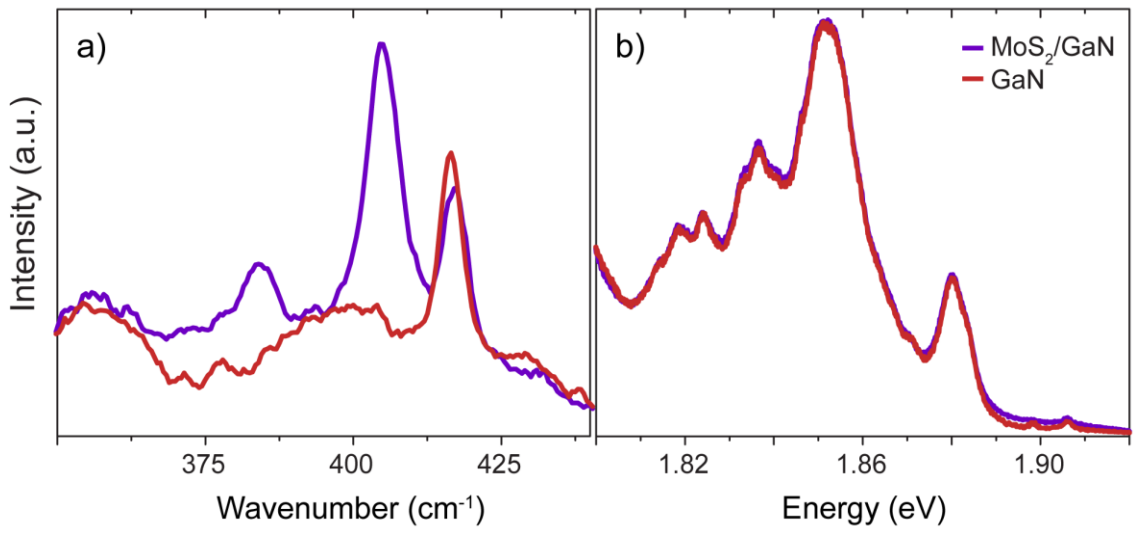

Figure 3.12: Raman and photoluminesence of 5L-MoS_2 grown on treated *n*-GaN surface and a bare treated *n*-GaN surface.

Another major benefit of performing the ammonia anneal in the MoS_2 growth chamber is we can grow MoS_2 on the pristine surface of GaN without breaking vacuum. The growth of MoS_2 occurs in this chamber at 650˚C and is thoroughly described and characterized by Kortney Almeida.[28] To transistion from the ammonia anneal to growth, the hotplate temeperature is lowered to 650˚C and gasses are switched from ammonia to H_2S, still with a pressure of $4x10^{-4}$ torr and growth occurs. Aiming for 4 layers of MoS_2 based on the studies done at Army Research Lab for the 3-terminal heterojunction bipolar transistor, Raman indicated 5 layers of material across the substrate. Figure 3.12 shows Raman spectra of the treated *n*-GaN and the 5L-MoS_2/*n*-GaN. MoS_2 peaks are located at

383cm^{-1} and 407cm^{-1}, which is a 24cm^{-1} seperation, indicating multilayer material. There is no photoluminesense that can be seen over the GaN/c-sapphire related peaks which is expected since photoluminesense is not present past the monolayer.

At this stage, it would be great to continue investigating the interface of MoS_2 and GaN with XPS. Unforunately at UCR, the XPS became unusable soon after the completion of the surface cleaning study. Despite this pitfall, we began to investigate the use of Low Energy Electron Diffraction (LEED) to investigate our interfaces.

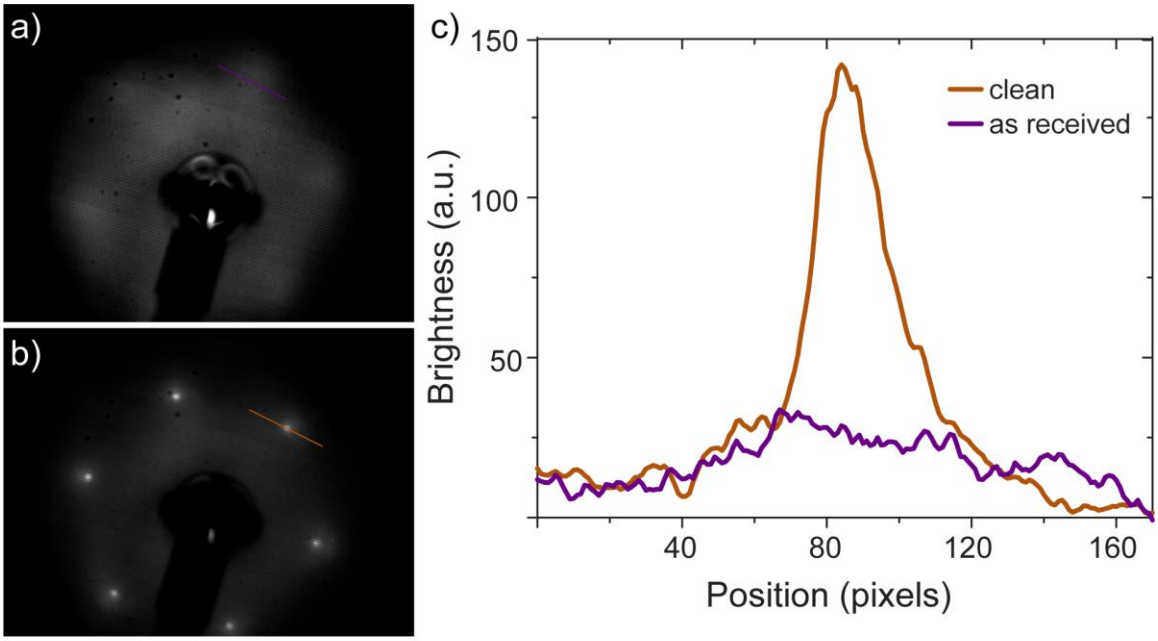

Figure 3.13: Low Energy Electron Diffraction (LEED) images of as received (a) and treated GaN (b). c) Plot Profile of brightness of LEED spot patterns.

To confirm our cleaning treatment for GaN, a simple experiment is performed. Looking at the as received sample in the LEED, we can see the emergence of the GaN peaks. They are cloudy and almost in the pattern of a ring, indicating a non-homogenous

and somewhat dirty surface. From previous XPS scans we know the surface has excess carbon and oxygen at the surface which we aimed to reduce in this study. After the complete GaN treatment, GaN LEED spots become much more bright and defined, indicating long range lattice patterns and a crystalline surface.

Ne Sputtering and NH_3 Annealing Investigation

Although we saw great improvement from the surface cleaning study thus far. We aim to optimize even more. In that effort, we explore the effect of neon (Ne) sputtering prior to the ammonia (NH_3) anneal. Sputtering has been proven to be a powerful tool on certain materials, commonly used as a type of cleaning method to eliminate the surface of any contaminates. Typical systems include argon (Ar) sputtering of Cu(111) surfaces for STM study.[88] In this study, we choose to use Ne^+ instead of Ar^+ since the primary contaimates we are concerned about are carbon and oxygen. Neon is in the same period as carbon and oxygen, therefore, is of similar size and atomic weight. Momentum exchange is most efficent for atoms of similar size and weight.[89] We expect sputtering with neon will be the most beneficial to our surface of GaN.

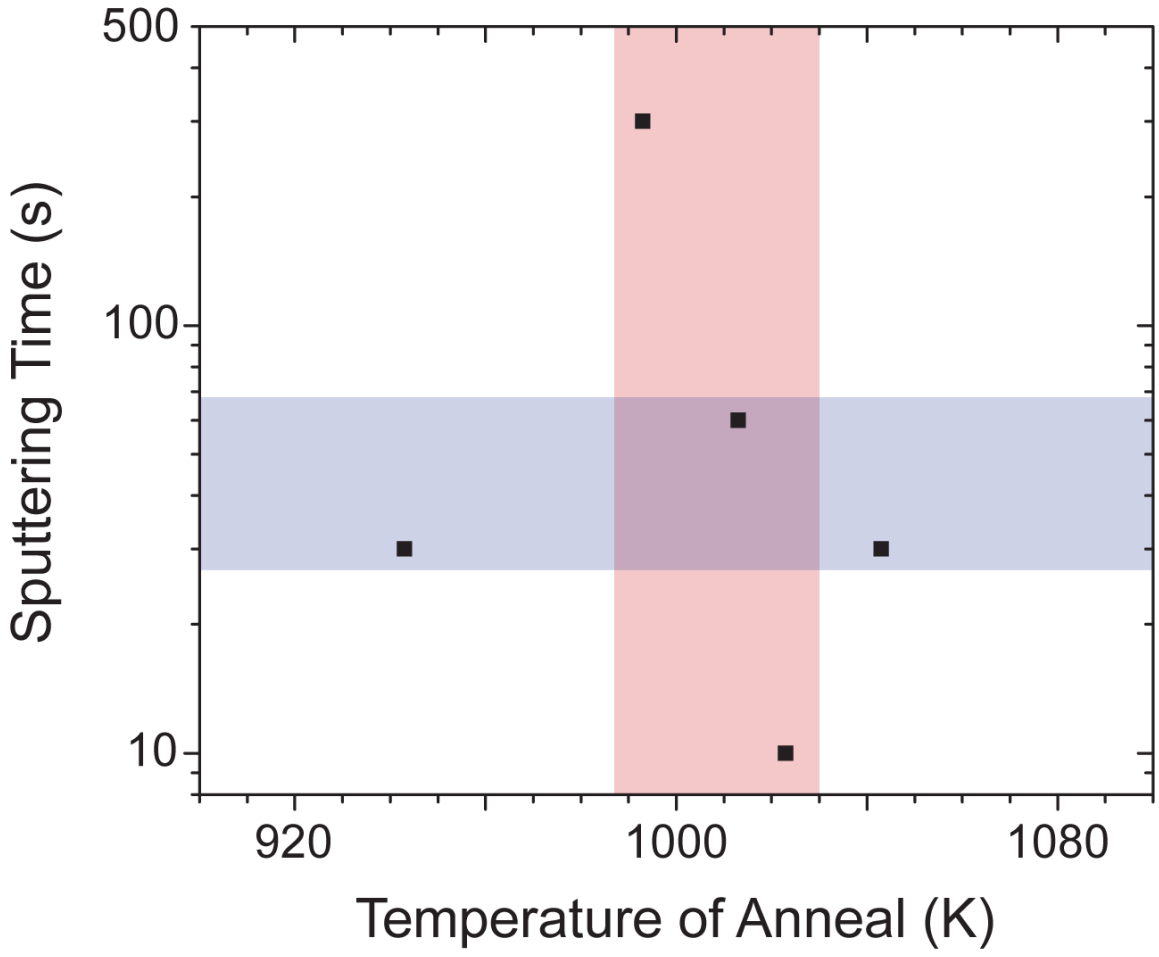

Figure 3.14: Total cleaning study of *n*-type GaN showing results of the combination of solvents, wet oxide etch chemistry, and a NH_3 anneal. Normalized to the Ga3d peak: a) Ga3d, b) N1s, c) valence band edge, d) O1s, e) C1s.

Figure 3.14 shows the parameter space explored during sputtering test of GaN. In each case, a full cleaning treatment is performed as described in the previous section prior to entering the MoS_2 growth chamber. We fitted a sputter gun onto the same chamber and directed it toward the GaN substrate. The Ne sputter treatment occurs in the chamber with a base pressure of $1x10^{-7}$ torr. Ne gas is leaked in to the chamber to a pressure of $1x10^{-4}$

torr. Using the sputter gun at 0.5keV beam energy and 2-3mA emission current, we expect our sputter to be gentle. We explore sputtering from 10-300seconds with various annealing temperatures to explore if we can maintain the nice surface we saw in Figure 3.14. Unfortunatly, none of these test produced LEED spots. This lead us to believe the neon sputter, despite the subsequent ammonia anneals, is damaging the surface so that it is no longer crystalline.

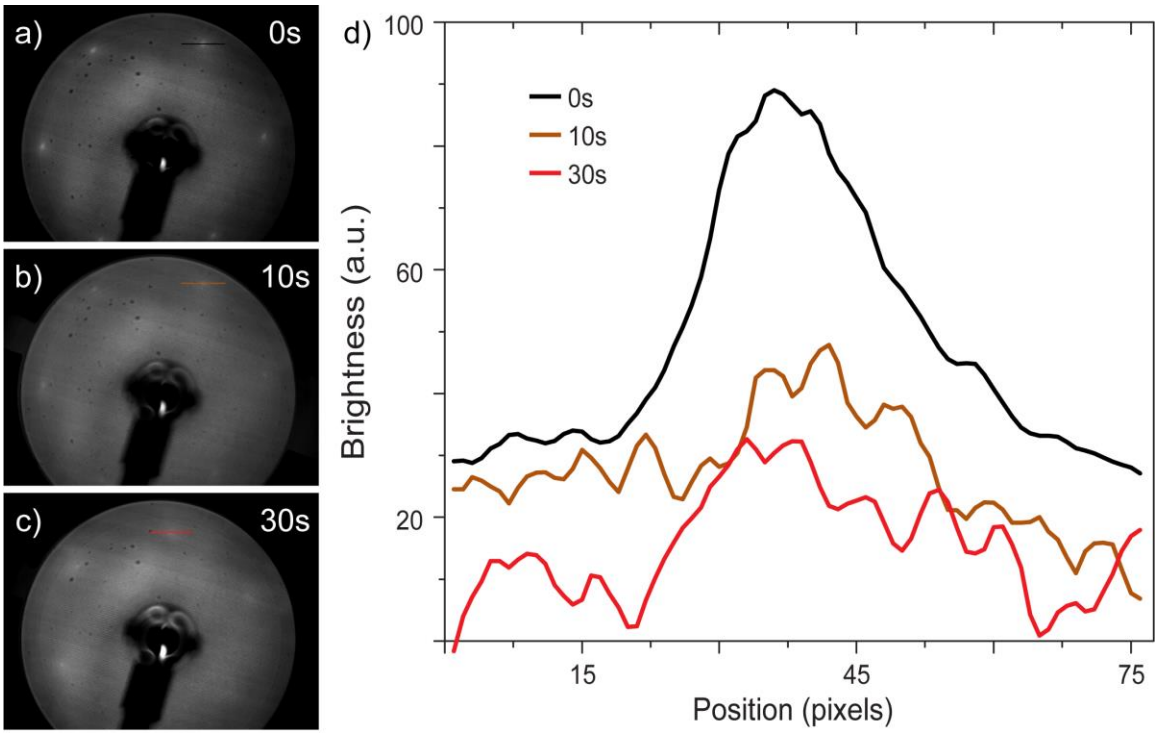

Figure 3.15: a-c) LEED images of sputtered GaN surfaces from 0-30 seconds. d) Plot profiles of brightness of LEED spots.

To show that is may be the case, we reduced our sputtering times to see if we can see how the LEED spots may be affected by sputter. Figure 3.15 shows results of LEED at lower sputtering time. We can see by broadening of the LEED spots, it seems we are doing

more harm than good to the surface of GaN. Even 10 seconds of Ne^+ sputtering seems to destroy the surface beyond repair by the NH_3 anneal.

Since we know sputtering works in other systems, we were curious to see if any amount of sputtering can lead to an impovement of the LEED spots which would be indicative of a cleaner surface. To do this, we developed a noval experiment where we can effectively sputter in a gradient across a sample. By mounting a metal shim in the growth chamber with a micrometer, we can effectively cover the sputter gun and release it to our substrate in increments. We decided since we can barely see LEED spots even at 30 seconds of sputtering our sputtering experiment should cover the range of the substrate over a time span of 30 sesconds. The LEED was fitted with micrometer stepper motors and controlled with an Arduino board through LabVIEW. The goal being to scan across the substrate which will have a gradient of sputtering time from 0-30 seconds and effectivly make a gif of images to see the effect. We realize this novel method of LEED analysis as shown in Figure 3.16.

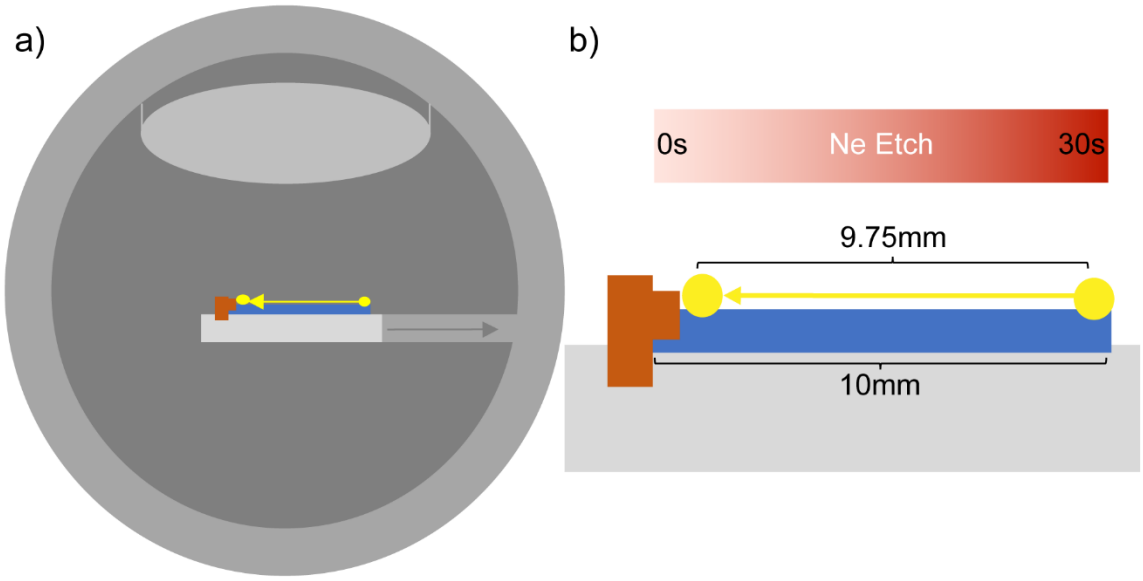

Figure 3.16: LEED setup for gradient sputter samples. a) LEED chamber stub with sample. b) Zoom of stub with sample and basic measurements of what we can measure without the beam being partially off the substrate.

Not only can we observe how GaN is affected by this method, we can do the same experiment by growing MoS_2 on top of GaN after sputtering to see if MoS_2 epitaxial growth is affected by the roughing of the surface of GaN. This way we can detemrine if there is an ideal amount of sputtering that can improve the surface.

Using a python code in conjunction with ImageJ software, batch analysis can be modeled over time.[90] Figure 3.17 is the output of that data. In each case, LEED spots and background data are selected and substracted.

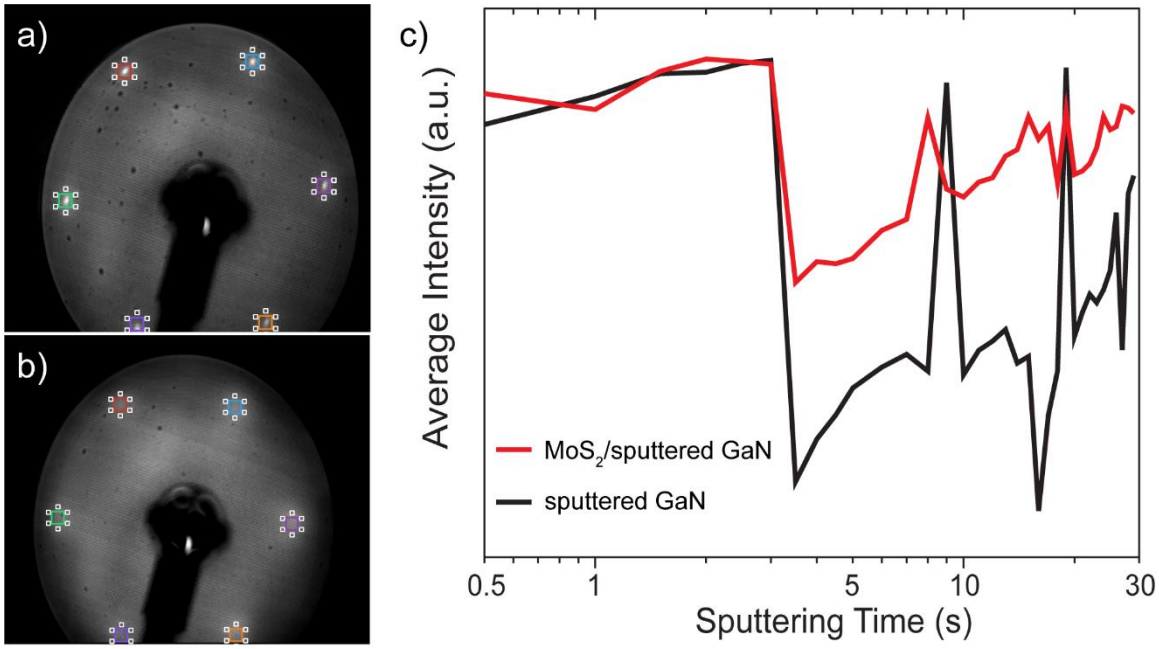

Figure 3.17: a) LEED image and analysis of gradient sputtered GaN. b) LEED image and analysis of MoS_2 on the gradient sputtered GaN. c) Average brightness amoungst the 6 spots with background substrated vs sputtering time.

In both experiments, it seems that there is a minor improvement of the LEED spots average brightness in the span of about 2.5 seconds. Soon after the 2.5 seconds, we see a sharp decrease in the average spot brightness followed by sharp spikes. It is unclear what the sharp spikes reference, however, it is clear GaN is very sensitive to sputtering. In my reccomendation for future work, one would be advised to avoid sputtering GaN and the previous treatment should be sufficent.

Conclusion

Two-dimensional materials, especially transaction metal dichalcogenides, have shown a wide variety of applications and variability of desirable electronic characteristics. Natively indirect band gap semiconductors, TMDs at the single layer exhibit direct band gaps suitable for optoelectronic applications. From a wide range of bandgaps, $MoTe_2$ (1.1eV) to WS_2 (1.95eV), TMDs can complement the properties of 3D semiconductors through their mobility and carrier concentrations along with potential lattice matching of materials for epitaxial growth. TMDs have great potential for next generation electronics that have excellent durability.

Various methods have been demonstrated to deposit pristine monolayer flakes: top-down approaches such as mechanical exfoliation from CVT crystals and liquid exfoliation that can lead to 2D printing efforts, bottom-up approaches such as chemical vapor deposition. Each method having its benefits and downfalls. High-vacuum growth of TMDs had been demonstrated and perfected in the Bartels lab over the years to produce high-quality layer-dependent MoS_2.

Although monolayer TMD material is optimal for the maximum thinning of future electronics, synthesis of purely homogenous films is challenging. Rhenium disulfide (ReS_2) is a novel TMD that maintains a direct band gap and holds great promise for facile synthesis of TMDs in industry. Challenges in consistent growth and the absence of ohmic contacts may slow the research on various TMDs. Raman spectroscopy proved itself to be a powerful tool and exposed there is more work to be done on exotic TMDs.

TMD thin films have many distinctive properties that make them attractive for various device concepts. Although a large part of the electron device community is attracted to TMDs for their direct band gap, they have proven to play a key role in advancing performance and high-power devices. Vertical devices based on 2D semiconductor heterostructures have the potential for high speed and large power performance. One could take advantage of mainstream 3D materials such as GaN and novel 2D materials such as transition metal dichalcogenides to fabricate this structure.

The path to a functionable 3-terminal heterojunction bipolar transistor (HBT) has been revealed. It was shown that clean, sharp interfaces play a major role in the electrical performance of proposed devices. A treatment method was developed and characterized via XPS and LEED for the growth of *n*-layers MoS_2 on GaN at the University of California, Riverside.

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Appendix

Cleanroom Tools

- Deposition
  - Ebeam Evap
    - ARL: ChA, Evatec BAK 641
    - UCR: Temscal BJD 1800
  - Thermal Evap
    - ARL: Kurt Lesker PVD 75 (ARL)
  - ALD:
    - ARL: Kurt Lesker 150LX ARL (+plasma)
    - UCR: Cambridge Nanotech
  - PECVD
    - ARL: PlasmaTherm
    - UCR: PlasmaTherm 790
  - Sputter
    - ARL: AJA ATC 22000 Co-sputter
    - UCR: AJA ORION 5, Temscal BJD 1800
  - Thermal CVD (dry and wet oxides)
    - UCR: tube furnace
- Etching
  - RIE
    - ARL: Ulvac NE500e
    - UCR: STS Multiplex
  - ICP
    - ARL: Ulvac NE500e
    - UCR: Oxford Plasmalab 100/180
  - Wet Etches
    - ARL/UCR: BOE/HF
    - ARL/UCR: KOH
    - ARL: AZ500MIF
    - ARL: Cu
    - ARL: Ni
    - ARL: Au
  - DRIE
    - ARL: PlasmaTherm 770 Silicon DRIE (Bosch)
- Other Tools
  - Ashers UCR/ARL
  - ARL: RTA
  - ARL: probe station
- Lithography
  - Photo

        - ARL/UCR: Karl Stuss M6 Mask aligner
    - Ebeam
        - ARL: Vistec EBPG5000+ES
        - UCR: Zeiss SEM Crossbeam
- Characterization
    - SEM
        - ARL: Ziess Auriga+EDS
        - UCR: Ziess Leo SUPRA 55
    - AFM
        - ARL: Veeco Nanoman
        - UCR: Veeco Dimension 5000
    - Height Profile
        - ARL: Tencor P-15 Profilometer
        - UCR: Veeco Dektak 8
    - XPS: ARL/UCR
    - Ellipsometry UCR